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An HF Vector Network Analyzer – Part 1

You can have most of the performance of the high-priced spreads at a fraction of the cost!

This will be a three-part article that describes a homebrew vector network analyzer (VNA) for transmission and reflection measurements from 0.05 to 60 MHz., with optional narrowband extensions for measurements through 500 MHz. This VNA requires an IBM compatible PC and uses custom software.

This VNA and its documentation are aimed at the serious experimenter with a basic understanding of transmission lines. An understanding of scattering (S) parameters would be helpful as well. This VNA can be replicated by anyone with moderate skills in surface mount technology.

This part describes some measurement examples, theory of operation, and a performance summary. Part 2 contains the schematic, PCB, construction, support circuits, and acknowledgements. Part 3 will deal with the software, general usage, and narrowband extensions to VHF and UHF.

Some Measurement Examples

Before describing the VNA in detail, five measurement examples are presented to give an overview of what this VNA, and VNAs in general, can do.

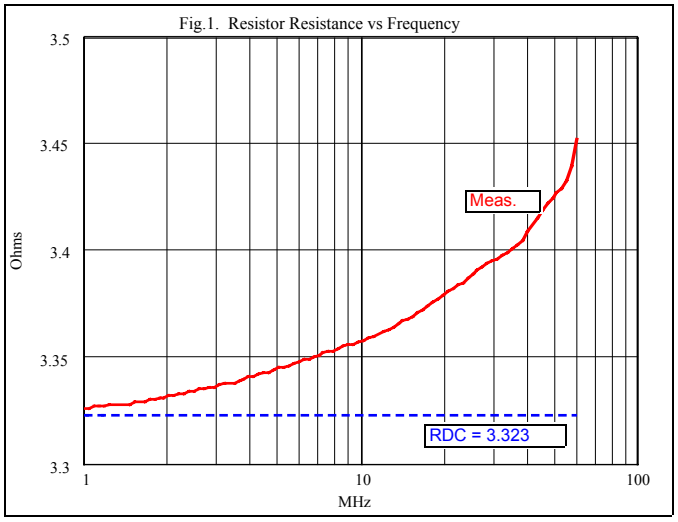
Series RLC Network

This example illustrates the VNA's reflection measurement capabilities. Unlike instruments that infer the sign of the reactance (sometimes incorrectly) from impedance trends with frequency, a VNA is able to make this determination from data at a single frequency. The complex reflection coefficient is measured and then related impedance and other data are calculated.

The components are:

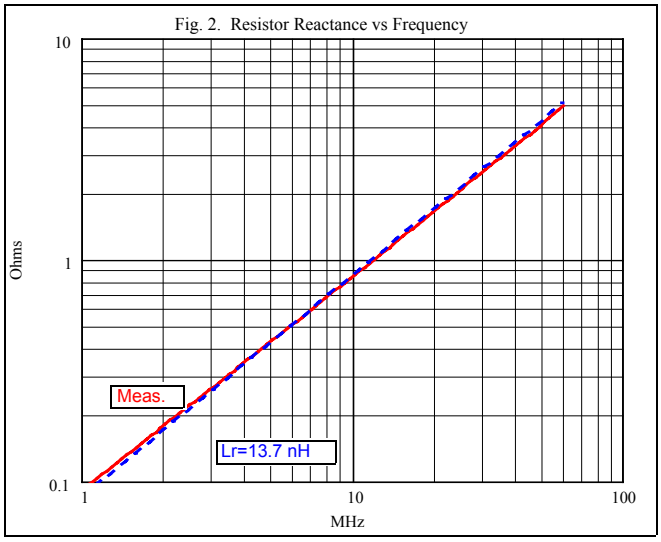
- 3.3 Ω,1/4 w, +/-1%, axial-leaded metal film resistor, one inch overall (lead + body) length
- 150 pF, +/-5%, 500 WVDC, mica capacitor, one inch overall (lead + body) length
- Nominal 10 uH inductor, 28 turns, #24 AWG enameled, T37-3 toroid

Lead lengths were intentionally made relatively long to demonstrate the VNA's ability to determine the associated stray inductance, predominant in these cases.



Each component was characterized independently and the series combination of all three as well. Data was collected at 100 logarithmically spaced points from 1 to 60 MHz.

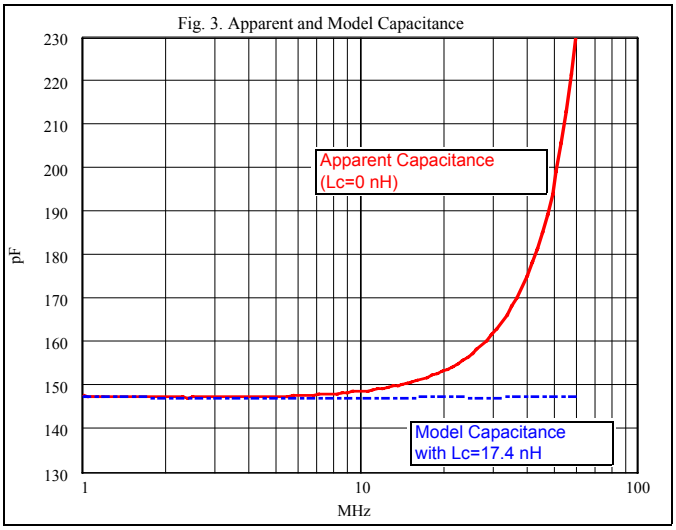
The measured and modeled series resistance and reactance vs. frequency results for the resistor alone are shown in Figures 1 and 2.



There is good correlation at 1 MHz between the resistance measured there and a 4-point Kelvin probe DC resistance measurement. There appears to be skin effect and proximity effect dependencies of resistance with frequency. Note however that the total change in resistance is only 130 milliohms.

Figure 2 shows good correlation of resistor reactance to an ideal 13.7 nH inductance, which is reasonable for a 1 inch long wire about 1/8 inch over a ground plane.

The measured and modeled results for the capacitor alone are shown in Figure 3. The apparent capacitance is determined assuming the stray series inductance is zero which

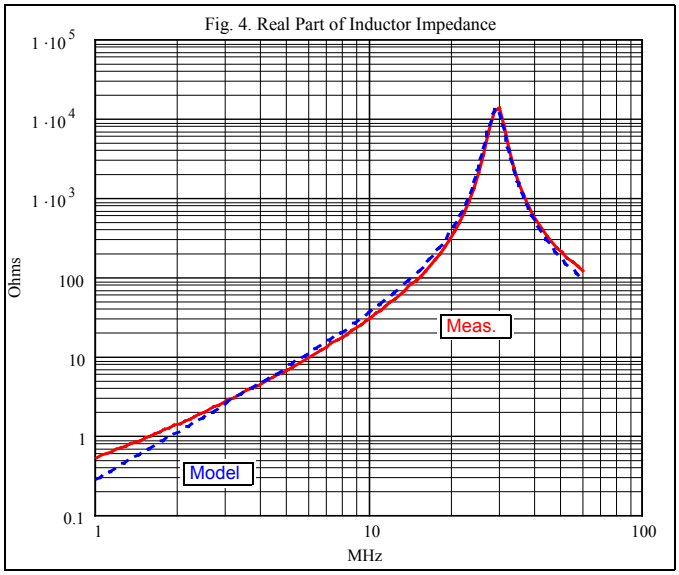


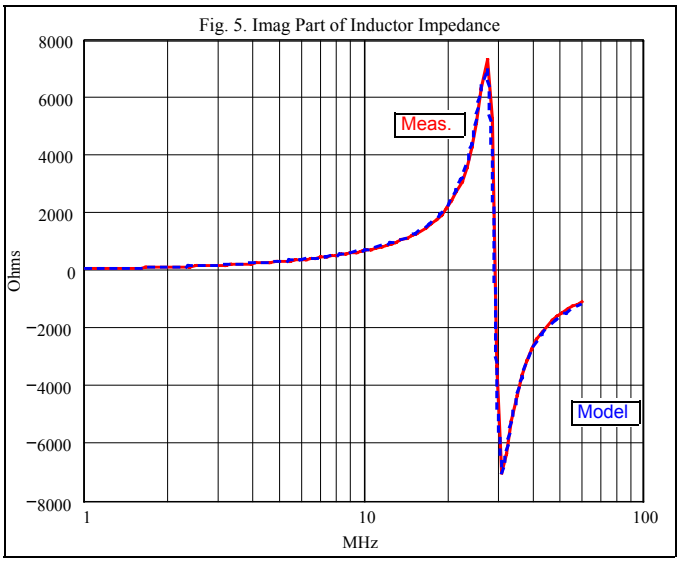
it clearly is not. The effect of series inductance is to lower the overall measured reactance at any given frequency and hence results in an apparent capacitance that increases with frequency.

A series inductance of 17.4 nH results in a capacitance that is essentially independent of frequency, as seen in Figure 3. So a more accurate model for this component would be 147.2 pF in series with 17.4 nH. Even though the lead lengths are the same for resistor and capacitor, the resistor is closer to the ground plane and hence has lower loop inductance.

Capacitor Q would also generally be of interest. But Q exceeds 1000 in this case and such high Qs are not very reliable in this reflection measurement of the capacitor alone.

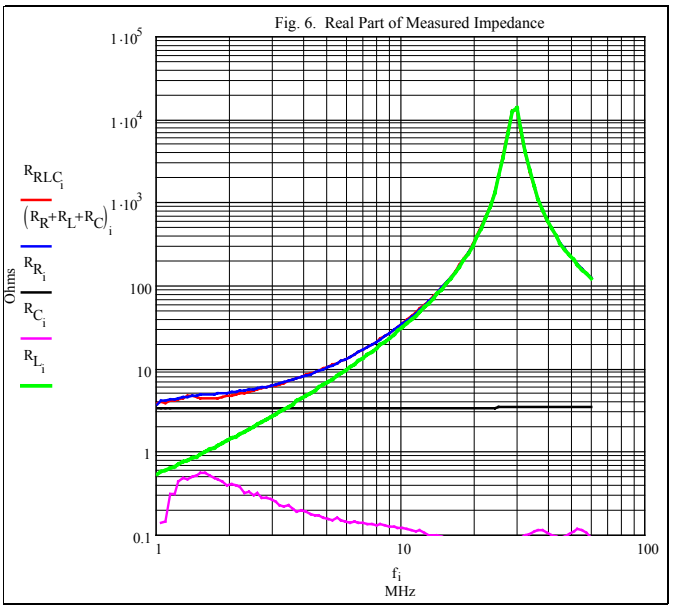
The measured and modeled results for the inductor alone are shown in Figures 4 and 5. Also shown are the real and imaginary parts of the impedance for an approximate model for the inductor consisting of a shunt combination of 14100 Ω, 10.03 uH, and 3.0 pF.

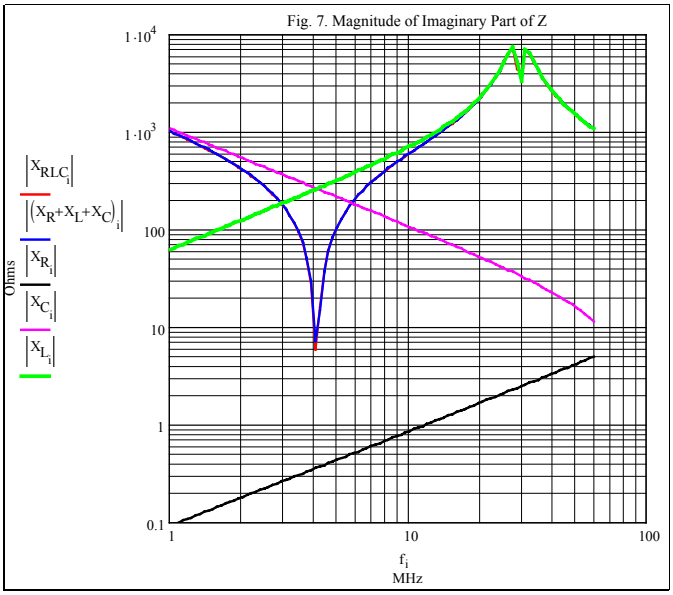




The model for the inductor is consistent with measured data over most of the 1-60 MHz range, including well above the parallel resonance at 29 MHz. Below 2 MHz, there is an increasing error in the real part of Z.

The measured results for the individual components and the series combination of all three are shown in Figures 6 and 7. Also shown is the algebraic sum of the individual component measurements, which is virtually indistinguishable from the measured series combination.





The observed series resonance is at 4.126 MHz vs. the calculated resonance at 4.135 MHz for the individually modeled components.

The series combination was ordered as LRC (capacitor grounded) to obtain the best agreement with the individual components, in particular near the inductor parallel resonance. This is judged to be primarily related to increased stray capacitance presented across the inductor near its parallel resonant frequency with alternate arrangements. More detailed models of each component would require the addition of lead to ground capacitances.

There is an almost complete absence of scatter in the measured data over nearly five orders of magnitude in R and |X|. While data scatter is only one of several elements that comprise accuracy, accuracy can certainly not be better than the scatter.

Scatter is mostly observed in Rc, which is related to the high capacitor Q. With such high Qs, reflection coefficients are near unity in magnitude. Random measurement error can cause |rho| to exceed unity in some cases with the apparent result that the component is better than lossless - one does

have to be careful when interpreting VNA measurement results!

Decoupling Capacitors

The second example is also a reflection-based measurement - of capacitors typically used for decoupling of power supply voltages near active circuits. Each capacitor was characterized independently and in various parallel combinations as well. Data was collected at 100 logarithmically spaced points from 50 kHz to 60 MHz and demonstrated the VNA's utility below 1 MHz.

The capacitors are:

- 10 uF, 16V radial-leaded aluminum electrolytic capacitor
- two 0.1 uF axial-leaded ceramic capacitors
- 0.01 uF ceramic disk capacitor

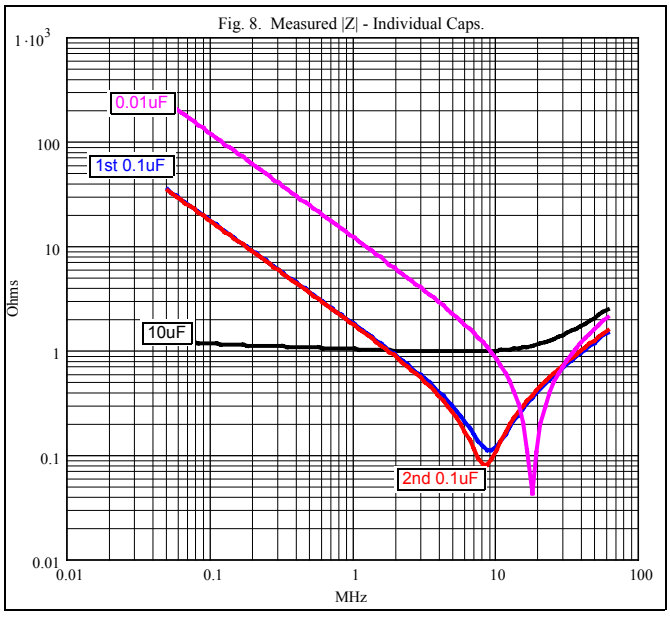
All components were approximately 0.45 inch overall lead plus body length.

The electrolytic capacitor was initially measured using a bridge that allowed the capacitor under test to be biased from 0 to 15V. These tests showed that the capacitor |Z| varied very little over this bias range. As a result, the data presented here was collected using a conventional return loss with the capacitors unbiased (0 VDC).

As is the convention for decoupling capacitors, the magnitude of the impedance (|Z|) is plotted here vs. frequency. However, the file data also contains the real and imaginary parts of Z, which are used as needed.

Figure 8 shows the measured |Z| for the individual capacitors. Except for Cs and Ls of the 10 uF, the following parameters can be approximately deduced from Figure 8 for each capacitor:

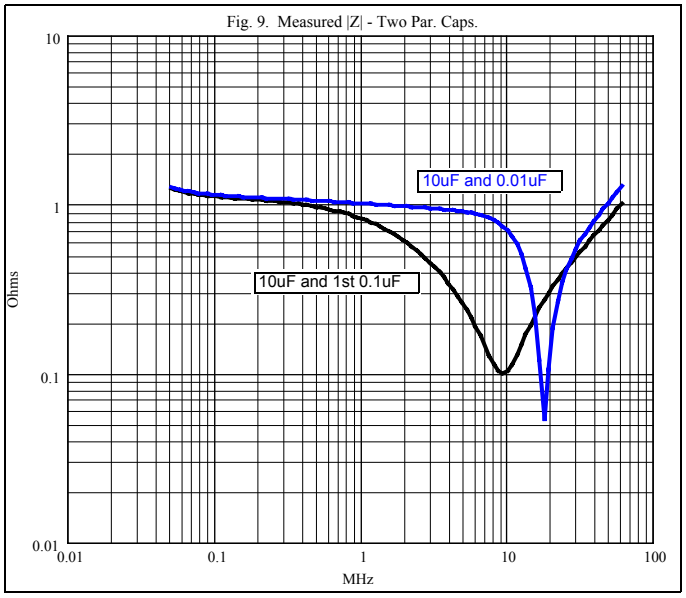
Nominal	Cs	Rs	Ls
10 uF	6.0 uF	0.99 Ω	6.3 nH
#1 0.1 uF	0.0915	0.11	3.7
#2 0.1 uF	0.0933	0.08	3.9
0.01 uF	0.0136	0.04	5.9



Due to the dominant effect on |Z| of Rs for the 10 uF capacitor over most of the plotted frequency range, the file data for Cs at 50 kHz and Ls at 60 MHz was used.

For the 0.01 and 0.1 uF capacitors, Cs is determined from |Z| at 50 kHz, Rs is the |Z| at series resonance which occurs at the respective valleys of |Z| (also 10 uF), and Ls is found by Cs and the frequency of series resonance. Alternatively, Ls can be determined from the file data based on Xs at 60 MHz; the values determined in that fashion are within 0.4 nH of the values determined from series resonance.

Next, certain two capacitor parallel combinations, selected based on broadband decoupling, were tested with the results shown on Figure 9.



As might be expected, the 10 uF in parallel with the 0.1 uF provides the better decoupling over most of the frequency range.

Last, certain three capacitor parallel combinations, also selected based on broadband decoupling, were tested with the results shown on Figure 10.

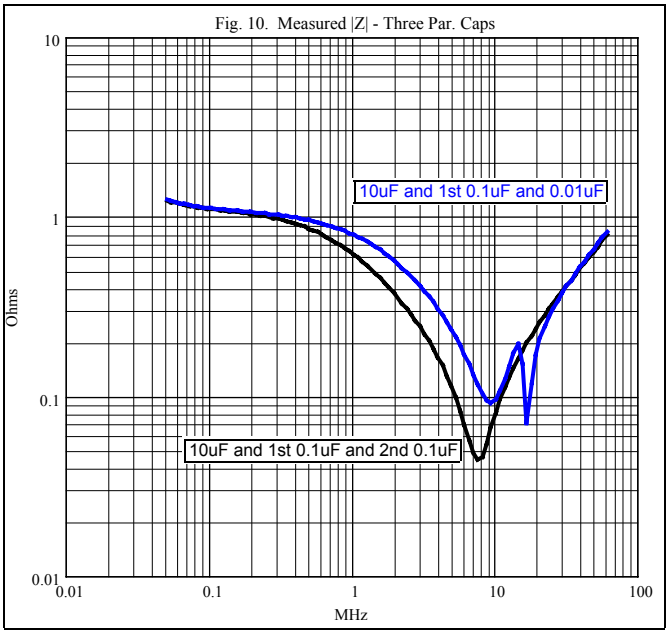


Figure 10 shows a pitfall that can occur with paralleling different value capacitors. The 10/0.1/0.01 uF combination shows first the series resonant valley at about 9.3 MHz due to the 0.1 uF, then a parallel resonant peak at about 14.3 MHz, followed by the series resonant valley at about 16.5 MHz. The extent of the actual impedance excursions is likely to be greater than shown due to the 1.2 MHz spacing between data points in this region. The parallel resonant peak primarily is the result of the series inductance of the 0.1 uF and the net

capacitive reactance of the 0.01 uF capacitor at the parallel resonant frequency.

Instead, the 10/0.1/0.1 uF combination provides better decoupling over most of the frequency range, except for a narrow window from about 15 to 30 MHz.

The two capacitor combinations in Figure 9 do not show a similar parallel resonant peak due to the relatively high Rs of the 10 uF capacitor which results in a much lower Q resonance.

Single Band Antenna Matching

The third example is also reflection based and illustrates this VNA's ability to remotely measure impedance at high VSWR (low return loss).

The antenna is a vertical with an 11.6m overall height and a limited ground screen. There is a 2 foot piece of RG-8 coax to the antenna. PL-259 connectors are used on the antenna coax and the buried coax run back to the rig and serve as the interface to any matching units to be used. The single-band matching units for this antenna will be simple fixed component LC units, each with a pair of SO-239 connectors.

The general method used here is:

- Measure the antenna feed point impedance at a desired center frequency.
- Calculate the component values of a circuit that matches to 50 Ω coax.
- Select/build and measure the components at the center frequency.
- Check the expected match quality based on the measured components.
- Assemble the matching unit, place it at the antenna feed point, and measure input Z and VSWR.

The VNA was calibrated using homebrew PL-259 Open/Short/Load (OSL) standards located at the antenna feed point. Essentially, these calibration standards establish the VNA reference plane at the interface between the antenna coax and its PL-259 connector. The end use coax run was used for this measurement so that the VNA could remain on the bench.

A precise understanding of reference plane location is essential to perform and analyze the results of the most demanding VNA testing - even at 1.8 MHz. Also, careful construction, usage, and maintenance of calibration standards is essential to obtain the best possible VNA accuracy.

At 1.82 MHz, the measured Z = 7.04 - j577.2 which corresponds to a return loss of 0.018 dB, |rho| = 0.9979, and an VSWR of 953:1 - a challenge indeed to match in a low loss fashion and a good test of VNA measurement accuracy!

The series L and shunt C configuration was chosen for this matcher. In this case, the C is on the rig coax side. However, with such a high Z and VSWR, stray capacitance on the antenna side also had to be accounted for. This was initially estimated to be about 5 pF.

MathCAD was used for the calculations. Component Q was also included in the calculations. Initially, inductor Q was estimated at 450 based on Amidon data for the T200-2 core and a capacitance Q of 1000 was assumed.

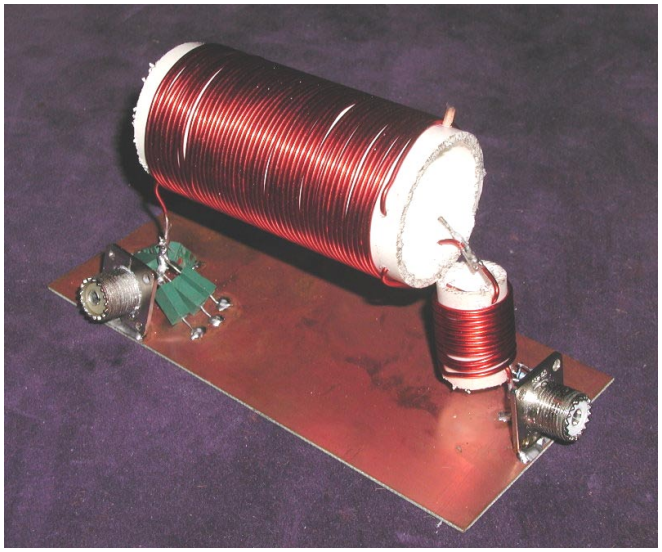
The results of the MathCAD calculations are:

- L = 50.458 uH
- C = 4040 pF
- Total loss = 0.74 dB

The inductor was initially constructed on the T200-2 core, but was found to have minor variations in inductance with power level from 50 mW to 100 watts and it also dissipated excessive power. As a result, a pair of inductors, close-wound on PVC forms, was used instead. The VNA measured L=50.1 uH and Q=250 for the pair in series. In this case, Q was measured with a 150 pF mica capacitor in series resonance, as a shunt impedance in a two port network to obtain better accuracy.

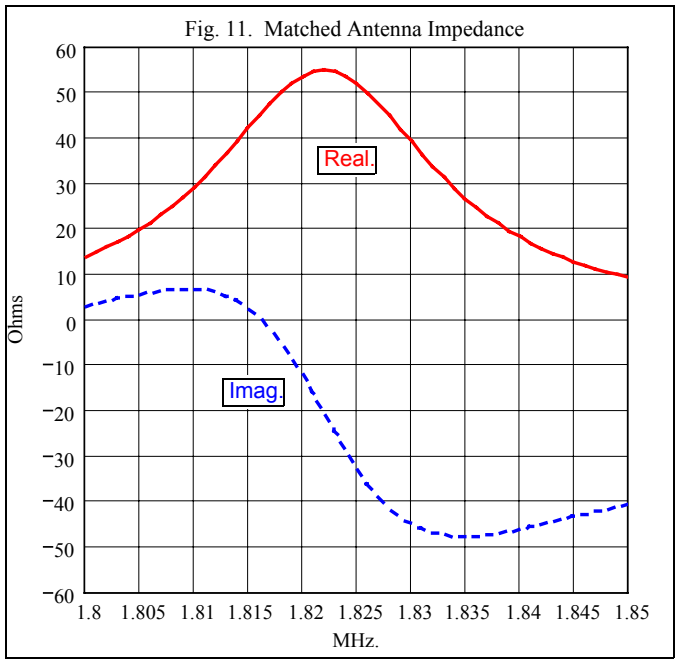
The capacitance is formed with eight 510 pF micas. The stray capacitance, due to the connectors on the antenna side of the matching unit, was measured at 4.4 pF. Since the inductor is now physically larger, the original estimate of 5 pF was increased to 6 pF.

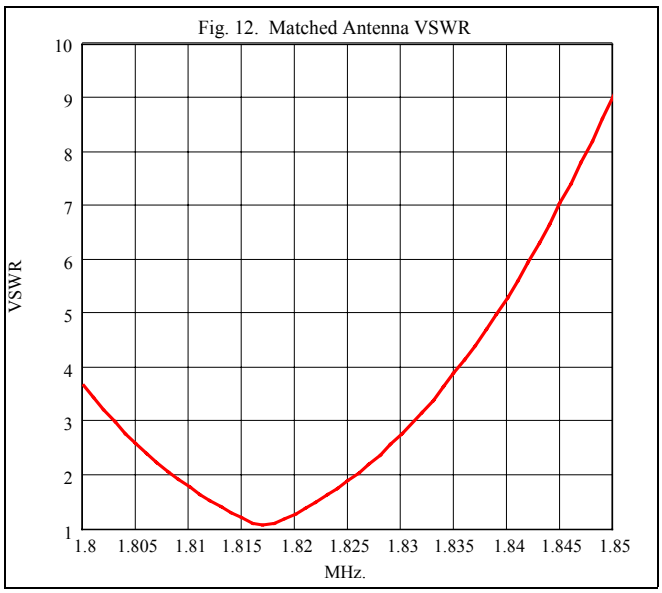
Here's a picture of the 160m matching unit:



Since there were some differences between the desired or estimated and the measured values, the MathCAD program was used to re-check the match using the measured and new estimated values. The predicted match was still good with VSWR=1.13 and return loss=24 dB at 1.82 MHz.

The results of the antenna with the above matching unit, at 1 kHz steps, are shown in Figures 11 and 12.





Clearly, a good impedance match has been obtained, quite close to the 1.82 MHz design point, without resorting to intentionally adjustable components. The 2:1 VSWR bandwidth is relatively low at about 18 kHz, which is typical for such relatively short antennas. Changing the spacing between turns on the larger inductor can also be used to move the minimum VSWR point to make this unit usable over the lower 40 kHz of this band which covers the author's interest here.

9 MHz FM Crystal Filter

A three-crystal noise filter was desired for a homebrew FM VHF receiver to filter broadband noise generated in the early IF stages. All components to be used in this filter are fixed value - no adjustable components were planned. The desired bandwidth is 15 kHz and the filter input and output impedances are 50 Ω.

First, the primary crystal parameters, determining series and parallel resonance, were calculated using the VNA measured data:

Unit	Rm	Lm	Cm	Co
10	14.4 Ω	13.3mH	23.5fF	4.4pF
19	13.0	12.4	25.2	4.6
35	13.8	13.1	23.9	4.3

The series resonant frequencies were within 370 Hz for these three units. In the interest of brevity, not all significant digits needed to accurately represent the series resonant frequency are shown above. Also not discussed are many details that are required to accurately characterize crystals.

A trial filter design was done in simulation and using Wes Hayward's software as a general guide. The transformers, for use in a 50 Ω environment, and other parts were measured using the VNA and the PSpice simulation model was refined using the new component parameters. The filter was constructed and measured for insertion loss and group delay vs. frequency.

There was some lack of correlation between measured and simulated results. This was found, in part, due to minor measurement problems where a pi model was needed for some components and not originally included. It was also estimated that the undesired close-in crystal spurious responses might be having a measurable reduction on filter bandwidth. So, the spurious crystal responses were then measured and their parameters were generated and included in the simulation model. Once that and the other component model changes were done, the simulation model came into very close agreement with measured data. From there, minor changes to two components were made using the simulation model and confirmed in a filter test to obtain a slightly wider bandwidth and equalized group delay distortion (GDD) at the ends of the filter pass band.

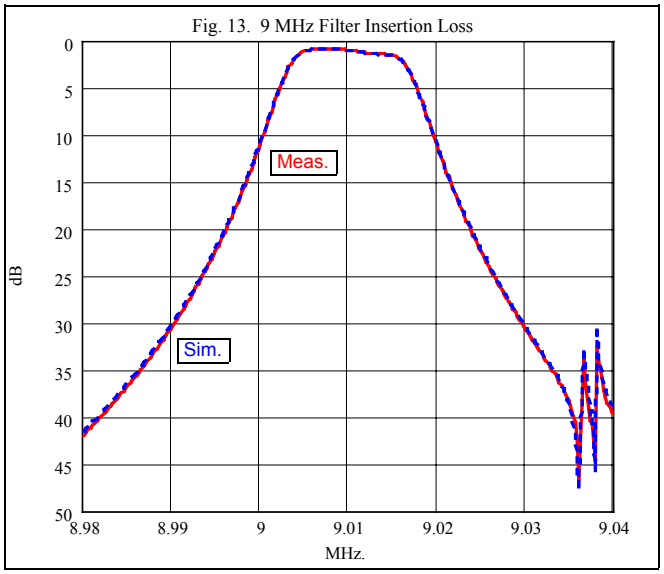
Here's a picture of the filter in its tested form:

To achieve the desired bandwidth, which is relatively wide for a ladder crystal filter, balanced transformers with neutralization capacitors are used on the end sections and a neutralization inductor is used in the middle section.

Here's a summary of measured and simulated filter parameters:

Parameter	Measured	Simulated	Units
Fo	9009.9	9010.0	kHz
IL	1.13	1.13	dB
3 dB BW	14.6	14.7	kHz
6 dB BW	17.0	17.1	kHz
GDD	23.4	23.3	us

In addition to the tabular data, the correlations between measured and simulated filter responses are also shown vs. frequency (250 Hz steps) in Figures 13 and 14.

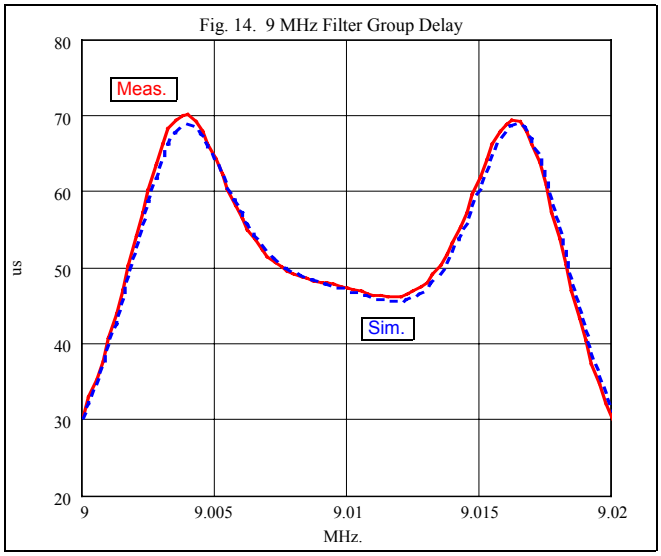


The correlation between measured and simulated insertion loss is quite good, even including the responses at the crystal spurs between 9.035 and 9.040 MHz.

Not shown here is the good correlation near the crystal spurs at 9.085 and 9.113 MHz with insertion loss peaks at 19 and 41 dB respectively. In actual usage, these spurious peaks will require that this filter be preceded by a higher order filter that will hopefully reduce the combined spurious responses to an acceptable level.

Group delay is typically of interest only around the filter nose and is plotted here over a narrower frequency range. As

with insertion loss, the correlation in group delay is quite good. Group delay, which requires accurate measurement of small



phase changes with frequency, is the more difficult of the two parameters to obtain accurately.

The correlation between measured and simulated filter data also demonstrates how the VNA data is internally consistent between its reflection and transmission measurement modes. This is the result of taking reflection based component data, putting that data into a simulation model that predicts filter transmission characteristics that, in turn, match VNA measured transmission data to a high degree.

F_t For a PN2222 Transistor

This last measurement example demonstrates full two port measurement of S-parameters on a non-linear device.

F_t is a measure of the gain-bandwidth product of the transistor. It is normally determined by the product of |beta| and the test frequency. That product is approximately constant when the test frequency places |beta| on the roll-off portion of its curve.

The transistor was configured as common emitter and biased thru a pair of 100 uH inductors - each 43 turns on a FT37-61 core. The inductors have a self-resonant frequency of about 20 MHz, which was desirable to minimize their effect on measured data. Inductor saturation was checked and was not found to be a problem up to 40 mA.

The VNA directly measures the two-port S-parameters, which are then converted to H-parameters. Measured F_t is the product of $|H_{21}|$ and the test frequency.

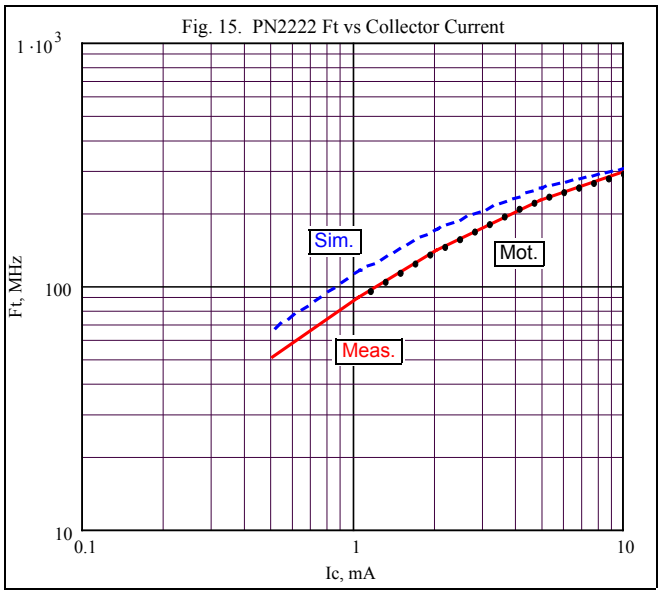
VNA calibrations were done at the transistor connection points using a piece of braid for the short, a 49.9 Ω chip resistor for the load, and a short wire jumper for the thru. Each port was left open for the open calibration load. The low frequency drive was reduced to about -42 dBm for S11 and S21 to maintain small-signal conditions.

Here's the measured and simulated results for a PN2222 at Vce=10 V and Ic=10 mA:

Test	F_t	
Frequency	Measured	Simulated
10 MHz	290 MHz	301 MHz
20	296	303
30	297	304
40	298	304
50	298	304
60	295	304

Both measured and simulated results support the expected 6 dB/octave roll-off of |beta| with frequency.

In addition, data was collected at Ic=5, 2, 1, and 0.5 mA. Figure 15 shows the comparison of measured and simulated F_t vs. collector current at a test frequency of 40 MHz. Also shown are Motorola data for the similar MPS2222 at Vce=20 V.



The correlation between the measured and the Motorola data is particularly striking. Normally there's a peak in F_t, but apparently the collector currents used weren't high enough for that to occur. The Motorola datasheet indicates that peak occurs at Ic=25 mA in this transistor.

Theory of Operation

There is much information related to general vector network analyzer principles available on the web [1] [2]. In particular, Agilent's AN1287-2 describes the typical VNA architectures. The referenced documents will be assumed as a base for what follows.

The key elements of a typical VNA are:

- A synthesized signal source that is voltage and/or software controlled.
- Couplers or bridges to separate incident from reflected signals.
- One or more receivers or detectors capable of amplitude and phase detection.
- Controls, data collection, and processing
- The Device Under Test (DUT), which can be a one-port or multi-port device
- Calibration (Reference and Calibration Planes)

The phase detection feature of the receiver or detector is what distinguishes a VNA from a scalar network analyzer (SNA). One example of an SNA is a spectrum analyzer with a tracking generator.

These elements of a VNA will be considered in further detail with reference to the block diagram shown on Figure 16. This diagram shows the essential elements of the printed circuit board (PCB) to be described in Part 2. One salient feature in Figure 16 is that there are no hardware calibration at a single frequency adjustments in this VNA.

How it Works – An Overview

Imagine a simple transmission measurement through a DUT (Fig 16). The RF DDS generates an RF voltage at the reference phase of 0 deg, and this signal is applied to the input of the DUT. The output from the DUT to the Detector input is an RF signal with amplitude $|V_{RF}|$ at a phase ϕ_{RF}. In addition, the RF signal at the Detector input is measured with a 'Through' in place of the DUT. The 'Through' is simply a short length of transmission line that is assumed to have unity gain and zero phase. The Detector output is also measured without any intentional RF signal at the Detector input. This test condition is referred to as the 'Open Detector.' For test flow reasons, the 'Through' and the 'Open Detector' measurements are made before the DUT is inserted and measured.

From these three vector measurements at a single frequency, all DUT transmission characteristics, such as gain and phase, can be calculated. Group delay requires two or more frequencies.

Similarly, all impedance characteristics of the DUT can be measured at each frequency of interest using a standard Wheatstone type reflection bridge. Here, the DUT $|V_{RF}|$ and ϕ_{RF} are measured relative to three precision terminations. The terminations are typically an open, a short, and one that approximates the system reference impedance (usually 50 Ω). These three calibration standards also allow the use of other measurement fixtures (not strictly bridges) that provide improved accuracy for high or low DUT impedances - see later.

$|V_{RF}|$ is quite easy to measure, but there are several different ways to determine the relative phase information θ_{RF}.

Most lab-quality VNAs use a superhet architecture that converts both the reference signal and the detected signal to a fixed IF for precision amplitude and phase detection. These conversions occur via conventional mixing or sampling. This architecture, as normally implemented, is complex and expensive.

A much simpler architecture is used in the recent 'VNA on a chip' device - the Analog Devices AD8302, with its broadband logarithmic detection of amplitude information and high-speed logic for the phase comparison. The disadvantage here is considerably reduced accuracy compared to a lab-quality VNA.

This VNA is different – it uses a narrow-band direct-conversion architecture that is much simpler than superhet VNAs, but is also much more accurate than the log-detection devices. Because the Detector in this VNA converts down to DC, the only output available is a DC voltage, which is dependent not only on the magnitude of the RF voltage at its input, but also its phase relative to the RF signal at its LO input. Highly accurate measurements of this amplitude and phase dependent DC voltage are obtained using a precision linear analog detector, a 24-bit analog-digital converter (ADC), and precise phase control of the LO DDS.

The phase information is obtained, in a novel way, by making two sequential DC measurements for each frequency and test condition (Through, Open Detector, and DUT). In each case, the first measurement is made with the LO at the reference phase of 0 deg; the second measurement is made with the LO phase shifted by 90 deg. This process results in the quadrature or vector components of each signal at the Detector RF input.

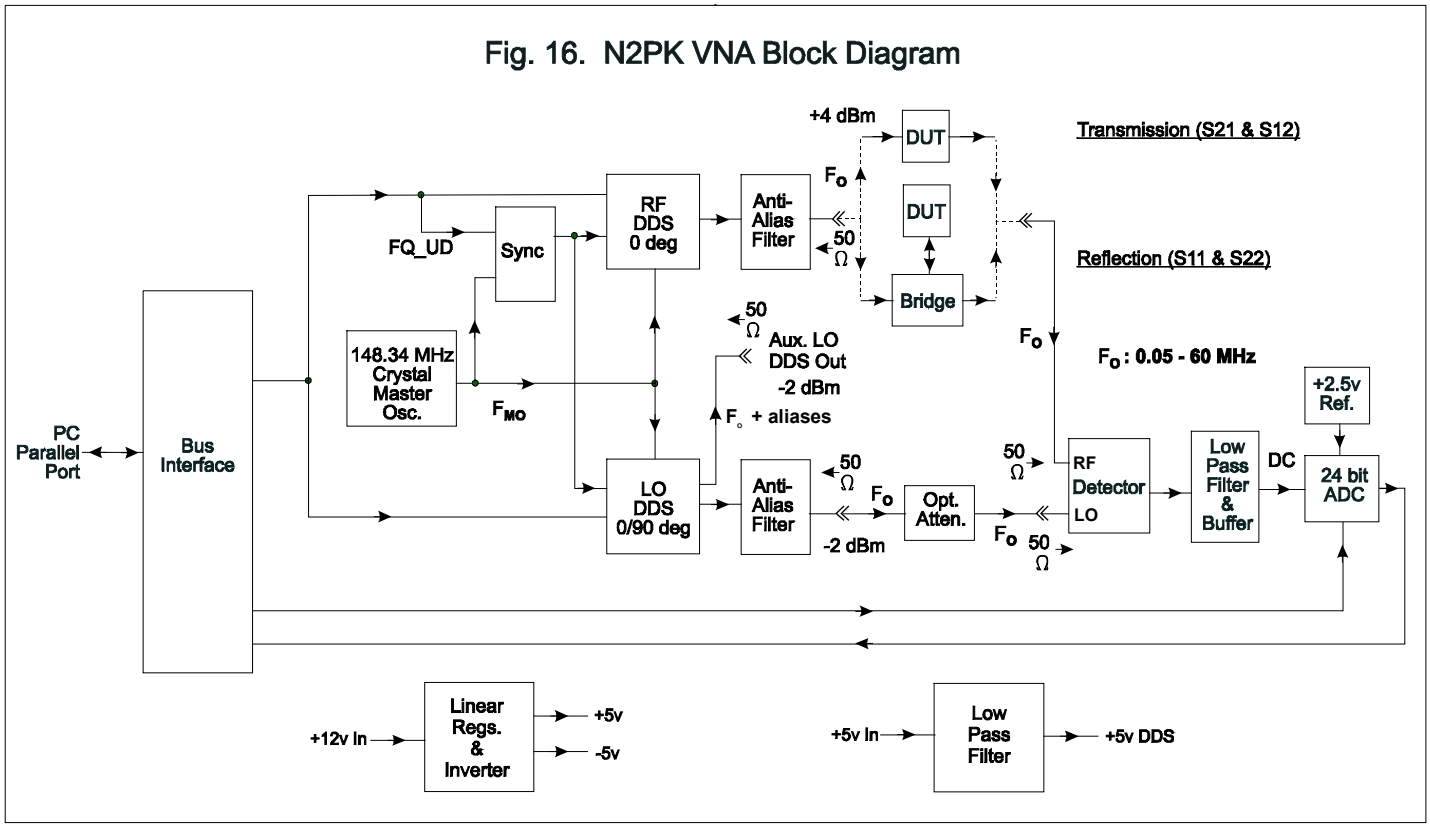
The result is a very simple hardware architecture, which takes maximum advantage of modern developments: the ability of a computer-controlled DDS to generate precise frequencies and phase shifts; precision 24-bit analog-to-digital conversion; and the power of computer control and post-processing. The computer processing completely eliminates setup adjustments, and allows many common sources of measurement errors to be 'calibrated out'. This greatly simplifies home construction.

Signal Source

There are two signal sources in this VNA. Both are based on direct digital synthesis (DDS) [3]. This reference supplies the general concepts of DDS technology and is assumed for what follows.

The RF DDS provides the signal source to the bridge and DUT during reflection measurements, or directly to the DUT for transmission measurements. The output from either the bridge or the 2nd port on the Device Under Test (DUT) feeds the RF input of the Detector.

Fig. 16. N2PK VNA Block Diagram



The Detector is a balanced mixer (see later) and the LO DDS provides the reference phase signal to the LO input of the Detector.

In normal VNA operation, the LO DDS is frequency and phase synchronized with the RF DDS. Both DDSs operate at the same frequency, which nominally ranges from 50 kHz to 60 MHz with a minimum frequency step size of approx. 0.035 Hz. In addition, both are usable for non-VNA applications below 50 kHz, particularly the LO DDS which is not transformer coupled.

Each DDS can be phase programmed from 0 to 360 degrees in 11.25 degree increments. As seen in Figure 13, the RF DDS is always programmed for 0 degrees while the LO DDS is programmed for either 0 or 90 degrees in typical VNA usage. The motivation for these phase selections will be described in the Detector section.

A 148.34 MHz crystal oscillator provides the master oscillator for the DDSs. This oscillator also synchronizes the frequency update control line from the PC to ensure that the desired relative phase is maintained between the RF and the LO DDSs. The original intent in this VNA was to support the 6X mode in the DDS to permit the use of a master oscillator at a lower frequency, which would have been easier to implement. When in 6X mode, a PLL internal to each DDS is enabled to permit a 6X frequency multiplication and synchronization at about 147.5 MHz, with only a 24.6 MHz master oscillator as input. However, three problems arose. The first was that amplitude and phase jitter was higher at certain frequencies with the DDS PLLs enabled. As a result, VNA measurement accuracy suffers, particularly near 24.6 MHz where the programmed frequency is within a few tuning words of 2AAAAAAAh, or about the internal master oscillator frequency divided by six. The second was that recently available documentation [4] indicates that both modes cannot be easily supported by one hardware configuration. This explains the intermittent software difficulties noted while attempting to operate in 6X mode with hardware designed for 1X mode. The third was that support of both modes was becoming increasingly difficult, as more software was being written and requiring test. As a result, support of the 6X mode was dropped in favor of a stable, low-noise crystal oscillator that generates 148.34 MHz directly.

Even with the DDS PLLs disabled, there is increased amplitude and phase jitter at certain frequencies with the largest increase near the 55555555h tuning word, which corresponds to the master oscillator frequency divided by three, or about 49.45 MHz. The jitter increases are caused primarily by an inverted alias that is in the Detector bandwidth, about –45 dBc, and modulates the detected amplitude. While these largest jitters amount to about a worst-case +/-0.2 dB uncertainty in transmission magnitude, or about +/-1.0 degree uncertainty in phase, and both are small for some purposes, the master oscillator frequency is selected so that jitter increases do not occur at 'round' number frequencies.

Anti-alias filters are provided on each primary DDS output to reduce the spurious DDS outputs above the Nyquist frequency. These filters start rolling off at about 50 MHz.

All DDS outputs are nominally reverse terminated in 50Ω, over a frequency range defined by AC coupling at the low end and an anti-alias filter, where present, at the high end. External 50 Ω attenuators (pads) can be used to improve source match at the expense of dynamic range.

To permit other uses of the VNA hardware, the DDS controls were configured to allow independent frequency control of each DDS. The auxiliary LO DDS output was not provided with an anti-alias filter to conserve board space and also since this output is not required for primary VNA functions. However, one can be easily added externally to support other uses, if desired.

Most commercial VNAs provide RF output level control. In the interest of simplicity, that feature was not provided here and can be readily supplied externally as needed with an attenuator.

Couplers and Bridges

There is a wide variety of devices that can be used here, but the requirement is always the same – to provide a measure of the signal reflected from a port on the DUT. A sampling of devices that can be used is:

- Return loss bridge [5]
- Two-way power splitter such as the Mini-Circuits PSC-2-1 or the PSC-2-1W [6]
- Directional coupler such as the Mini-Circuits PDC-10-1 [7]
- Two transformer directional coupler [8]

Bridges with high output impedances, such as the Bruene bridge, are typically not suited for VNA use, due to the VNA 50 Ω impedances.

For each of these devices, there are differences from the ideal for measures of the reflected signal. In all cases, however, the OSL calibration described below accounts for most sources of error.

While not generally considered a bridge, even something as simple as a 3-way tee connector directly connecting the RF DDS, the Detector RF input, and the DUT can be used. Unlike the conventional return loss bridge, this bridge is nominally 'balanced' when a short is placed on the DUT port, since the DUT shunts the RF DDS signal to ground so that little is available for detection.

Since this bridge is designed to make optimum use of the VNA's dynamic range for low DUT impedances, in Part 2 it is referred to as the "Low-Z" bridge. It is best suited for unbalanced DUTs, but the addition of a transformer can be useful for low impedance balanced DUTs, such as a loop antenna.

In similar fashion, the DUT can be inserted in series between the RF DDS and the Detector RF Input. This 'bridge' is balanced when an open is placed on the DUT port, since this DUT provides little signal for detection. In Part 2, this bridge is referred to as the High-Z bridge. This bridge is best used for measurements on physically small components since both DUT terminals are above RF ground, although a suitable transformer might be useful for unbalanced or balanced DUTs.

By AC coupling the RF DDS and DUT ports and DC coupling the DUT port and adding a bias resistor at the junction to a DC power supply, a simple Low-Z bridge can be built that allows testing of some active DUTs or bias dependent passive ones. This is much simpler, in most cases, than modifying one of the devices in the list above to accept DC biasing.

The combination of a Wheatstone type return loss bridge, the Low-Z bridge, and the High-Z bridge, with modifications as needed for DC biasing, can provide highly accurate measurements over a wide range of impedances.

Detector

This VNA utilizes a single Detector for both vector components of the RF input signal. It is a somewhat conventional linearized Gilbert-cell product detector (mixer) with a twist. Where a product detector is frequently provided with an LO (BFO) that is asynchronous with its RF signal and the information is contained in the detected sidebands, this product detector uses a synchronous LO and the desired information is in the detected carrier. Since the intermediate frequency (IF) in this case is zero Hz, the DC voltage at the Detector output contains the desired carrier information. This can be seen from Equation 1 that describes the Detector output voltage, V_{DC}:

$$V_{DC} = |G_{DET}| \times |V_{RF}| \times \cos(\phi_{RF} - \phi_{LO} + \theta_{DET}) + V_{off} \quad (1)$$

where, at each frequency,
$|\mathbf{G_{DET}}|$ is the magnitude of the Detector gain,
$|\mathbf{V_{RF}}|$ is the magnitude of the voltage at the Detector RF input,
$\boldsymbol{\phi_{RF}}$ is the phase at the Detector RF input,
$\boldsymbol{\phi_{LO}}$ is the phase at the Detector LO input,
$\boldsymbol{\theta_{DET}}$ is the phase constant related to Detector gain and,
$\mathbf{V_{off}}$ is an offset voltage with no applied signal at the RF input.

The absolute phase values for $\boldsymbol{\phi_{RF}}$ and $\boldsymbol{\phi_{LO}}$ are arbitrary since the reference for time is not specified. So, let's assume here that $\boldsymbol{\phi_{LO}}$ can be programmed to values of 0 and 90 degrees at different times. As a result, the Detector output takes on two DC values that together represent the quadrature or vector components of the applied RF signal within a vector constant, as shown in Equations 2 and 3.

$$V_{DC,0} = |G_{DET}| \times |V_{RF}| \times \cos(\phi_{RF} + \theta_{DET}) + V_{off,0} \qquad (2)$$

$$V_{DC,90} = |G_{DET}| \times |V_{RF}| \times \sin(\phi_{RF} + \theta_{DET}) + V_{off,90} \qquad (3)$$

The vector-offset voltage is obtained by measuring V_{DC} when V_{RF} is zero, i.e. with no input to the Detector. Its use in the computations is described below.

The LO DDS is connected to the Detector LO input in balanced fashion to minimize coupling back to the RF input, which is also balanced. The LO level is deliberately chosen to overdrive the Detector input, which makes its amplitude a second order effect that is accounted for principally in $|\mathbf{G_{DET}}|$, $\boldsymbol{\theta_{DET}}$, and $\mathbf{V_{off}}$.

To illustrate the application of equations 2 and 3 in this VNA, consider again the DUT transmission measurement.

At each test frequency and for each of the Through, Open Detector, and DUT test conditions:

1. Apply V_{LO} at the reference phase 0 deg, and measure $V_{DC,0}$ (equation 2)
2. Apply V_{LO} at the a phase of 90 deg, and measure $V_{DC,90}$ (equation 3)

The vector DC offset voltage, with components $V_{OFF,0}$ and $V_{OFF,90}$, is obtained from the Open Detector calibration, which is considered to result in $|V_{RF}| = 0$. The computer subtracts these values from all subsequent measurements.

With $V_{OFF,0}$ and $V_{OFF,90}$ known, the constants G_{DET} and $\boldsymbol{\theta_{DET}}$ in equations 2 and 3 are then implicitly determined with the 'Through' calibration. In actual fact, the measured values are converted to complex numbers to simplify the manipulations.

After the DUT measurement, standard complex number arithmetic is used to obtain the complex DUT gain, $G_{DUT,}$ in terms of the six measured Detector values expressed as three complex numbers:

$G_{DUT} = (M_{DUT}-M_{OPEN}) / (M_{THRU}-M_{OPEN}) = |G_{DUT}| \angle \boldsymbol{\theta_{DUT}}$

From G_{DUT}, expressions of magnitude as a real number and dB and phase in degrees are obtained. Group delay is determined from delta($\boldsymbol{\theta_{DUT}}$)/delta(f) using data at two frequencies.

Once collected, the Through and Open Detector calibration measurements can be used for subsequent DUTs as well.

A similar procedure is followed for reflection measurements using three calibration standards and the DUT. In this case, a separate no-signal measurement is not required to establish the Detector offset.

This method of vector detection is what I call *sequential quadrature* to distinguish it from the *simultaneous quadrature* done in other VNAs and real-time I/Q demodulators that employ two detectors and quadrature LOs instead.

While sequential quadrature is slower in terms of data collection, there are accuracy advantages due to gain and phase calibration tracking that results from the use of one detector and one LO that can be precisely phase shifted by 90 degrees. Note also that, in this configuration, absolute relative phase between the RF and LO DDSs is not at all important. Only the ability to precisely phase shift one DDS is critical to accuracy.

To further enhance accuracy, the detector DC output is processed as a differential signal, through to the differential input of the ADC. This provides valuable rejection of common-mode errors caused by thermal effects, power supply variation, and stray AC fields.

The Detector output is analog low pass filtered with a 3 dB cut-off at about 100 Hz (baseband). This filter is present to augment the ADC's Sinc digital filter, which has its 1st 3 dB down point at about 3.6 Hz. But the digital filter doesn't roll-off monotonically and has several large peaks at multiples of 15 Hz and at multiples of the 15,360 Hz sampling frequency (60 Hz notch frequency). For a 50 Hz notch frequency, these would change to 12.5 Hz and 12,800 Hz respectively. The analog filter time constant was selected to ensure that the Detector output settling time (about 14.5 filter time constants for 1 ppm) does not significantly increase the overall conversion time.

The analog filter output is also buffered by a pair of low offset, low drift, op amps to present an appropriate differential source impedance to the ADC.

The ADC is a differential input delta-sigma type with an integrated oscillator. The external voltage reference is differential to the ADC as well. ADC conversion time is relatively long at 130 ms, but that is the price paid here to obtain dynamic range on the order of 110-120 dB.

Based on measurements with an offset frequency on the RF DDS, the equivalent RF bandwidth of this Detector is about 5 Hz. So this Detector indeed qualifies as *narrowband*.

The return loss with respect to 50 Ω on the Detector RF input exceeds 30 dB over the HF range.

Since the data collected is vector in nature, averaging can be used to reduce the effective noise floor or effects of non-synchronous signals. While still subject to ultimate accuracy limitations due to drift, averaging can be helpful in some cases and the software allows the user to select the degree of averaging to be used.

Harmonic Mixing

One consequence of direct conversion and an over-driven LO Detector input is the potential for harmonic mixing. That can be used to advantage as one way to extend the frequency range of the instrument, but it can also result in undesired spurious responses. In particular, the 3rd harmonic can result in significant responses that may be either desirable or not. Desirable harmonic mixing will be considered in Part 3, but for now, we will consider the general mechanism and its effect on undesired responses.

For example, consider a filter designed for low insertion loss around its passband center frequency, Fc. Due to the over-driven Detector LO input, RF DDS harmonics, and potential harmonic generation within the DUT, a spurious response centered on Fc/3 will occur. That response can be about 80-90 dB down from the main filter passband response, neglecting the DUT contribution, and even higher if the DUT is a significant harmonic generator.

This is the result of the 3rd harmonic of the RF DDS passing through the filter passband essentially un-attenuated and mixing with the 3rd harmonic of the DDS LO. Due to the overdriven Detector LO input, 3rd harmonic mixing is only about 11 dB less efficient than fundamental mixing.

If the filter's response near Fc/3 is 60 dB down from the passband response, then the spurious response due to harmonic mixing will have a negligible effect. However, if the filter response is 100 dB down at Fc/3, then the spurious response will be seen as miniature passbands 1/3 as wide and centered on Fc/3.

If a suspicious response is seen, then an attenuator can be added to either the RF or LO DDS path to aid in determining its location.

If known attenuation between the RF DDS and the DUT results in higher relative measured attenuation at some frequencies, then this can be due to harmonic generation in the DUT. In this case, attenuation must be added until the desired linear response is obtained. This test only points to the DUT if the VNA Detector RF Input is not over-driven under any test condition.

Alternatively, adding an optional 20 dB attenuator between the LO DDS and the Detector LO input, as shown in Figure 16, will significantly reduce harmonic mixing. If a suspicious response is reduced in relative amplitude, then a VNA spurious response is indicated. While the spurious response can be reduced by over 25 dB to over 100 dB overall or better, there is a loss in dynamic range that is not generally desirable. This will dealt with in further detail in Part 3.

While a superhet approach in place of direct conversion would essentially eliminate the effects of harmonics (desired and undesired), a superhet would still be vulnerable to DDS aliases and now their other spurious outputs at frequencies more difficult to predict than the harmonics. A superhet and DDS clean-up using PLLs would result in a significant increase in hardware complexity with only a minor improvement in measurement accuracy in most cases.

Controls, Data Collection, Processing

Control over this VNA hardware is established via an interface to the parallel port on an IBM compatible personal computer (PC). The hardware does nothing without the PC and powers up “dumb.” In fact, warm-up of the unit doesn’t really start until one of the PC test programs has been started and the DDSs have been programmed to some representative frequency to be tested later after warm-up is complete.

The bus interface provides for ESD protection, has receivers with hysteresis for noise immunity, and has drivers capable of handling parallel port cables and loads per the IEEE 1284 standard.

The hardware is controlled by PC test programs which also collect the data from the ADC and perform subsequent data reductions to a variety of useful parameters. Several programs allow for stepping over a frequency range (spot, log, and linear), on-screen presentation of the reduced data after all collection is complete, and also data storage in a file. Other programs offer a quasi real-time capability at a single frequency with an on-screen and continuously updated display of the reduced data.

DUT

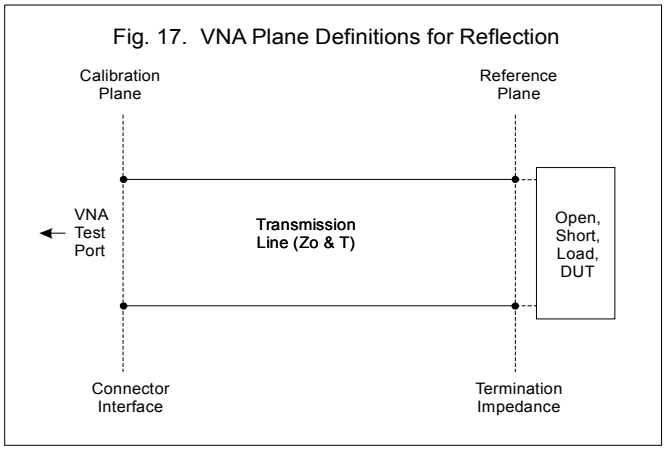
The Device Under Test (DUT) can be virtually any one, two, or multi-port network for which a linear characterization is useful. Care must be taken with some DUTs to avoid overdriving them and/or the VNA Detector. As noted above, an external attenuator can be used at the RF DDS to limit the drive to an acceptable level. In appropriate cases, the RF DDS output may also be amplified, but always subject to a maximum usable input of +5.5 dBm into the Detector as noted in the Performance Summary.

Calibration

An integral concept of any VNA is the *reference plane* [9]. For reflection measurements, the reference plane is the location on each DUT port where impedance is defined and is essentially defined by the location of the calibration standards and the DUT as shown on Figure 17. In addition, the *calibration plane* [9] is also defined, normally somewhere in the junction between the two halves of mating RF connectors.

One predominant usage of this VNA has been the precise characterization of components that are not associated with some particular connector system. Hence it is not particularly useful for the connector to be part of the DUT, particularly when the component impedances are much greater or less than 50 Ω. As a result, reflection data collected with this VNA currently are with respect to the reference plane.

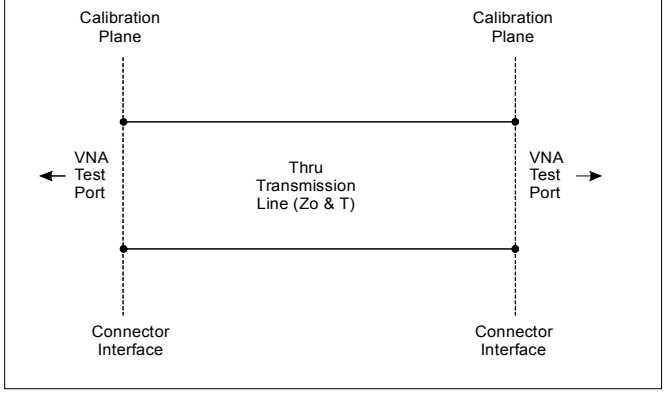
Fig. 17. VNA Plane Definitions for Reflection



For impedances thru 30 MHz with relatively low VSWR that are of interest at some particular connector interface, the differences between the impedances at the two plane locations are frequently negligible. However, for more demanding applications, the differences can be significant. At some time in the future, a choice may be offered to the user to define which plane is of interest for a particular measurement. This will also require of the definition of the parameters of the transmission line, normally its Zo and electrical length T, as shown in Figure 17. These parameters, which clearly also depend on the connector system used during calibration, introduce an additional level of complexity.

For transmission measurements of two or multi-port networks, the calibration plane locations for each port are individually defined as shown in Figure 18. The *Thru* line lies between the two calibration planes and thru 60 MHz would normally be characterized by Zo and an electrical length T (i.e. ignore loss). However, thru line parameters currently are assumed to be negligible since even something as large as an SO-239 to SO-239 barrel would result in only about 1.3 degrees of phase error at 30 MHz and about 1.8 degrees for an SMA-SMA barrel at 60 MHz. Again, this type of calibration refinement may be made in the future, but will require additional complexity and attention to detail by the user.

Fig. 18. VNA Plane Definitions for Transmission



This VNA lends itself to a full *Open, Short, and Load* (OSL) calibration for reflection measurements and a modified *Response* calibration for transmission measurements. These

calibrations are normally performed after warm-up, and immediately prior to measurement of the DUT.

OSL calibration basically views the entire VNA in reflection mode, from the reference plane to the ADC output as read by the PC software, as a linear two-port network. As such, this calibration accounts for what is normally termed *systematic* errors. *Random*, *drift*, and *non-linear* errors are not accounted for. The combination of drift and desired measurement accuracy normally determines how often calibration must be performed.

While four parameters generally characterize a two-port network, only three are required in this case since a numerical value for the product of two parameters is sufficient as shown in Eq. 4.

$$\rho_{meas} = E_{11} + \frac{E_{21} \times E_{12} \times \rho_{DUT}}{1 - E_{22} \times \rho_{DUT}} \qquad (4)$$

Hence, only three known loads are required to establish numerical values for E_{11}, $E_{21}xE_{12}$, and E_{12} at each test frequency. Armed with values for measured reflection coefficient, ρ_{meas}, E_{11}, $E_{21}xE_{12}$, and E_{12}, Eq. 4 can be used to solve for an estimate of the actual DUT reflection coefficient, ρ_{DUT}.

Conventional VNA *Response* calibration, used during transmission measurement of two or multi-port networks, requires a thru transmission line to establish a complex reference value at each test frequency for unity transmission in an assumed 50 Ω system. The *Modified Response* calibration employed in this VNA also accounts for the frequency-dependent DC offset present in the Detector with no signal applied at its RF input. This substantially increases the dynamic range of this VNA in transmission mode to make it comparable to that obtained with *Response and Isolation* calibration on tuned receiver VNAs (with non-zero IFs).

An analysis of an OSL calibration model that includes Detector offset shows that an additional calibration step is not required to account for Detector offset in reflection measurements.

Response calibration is not as accurate as full 12 error term two-port correction mainly because it does not account for source and load match in the VNA. But it is much simpler and quicker to perform. Its accuracy is acceptably good for most purposes since the source and load return loss in this VNA is better than 25 dB over the HF range (1.8-30 MHz). As noted earlier, external pads can be used where needed to improve transmission measurement accuracy. Judicious use of external amplifiers, on one or both sides of the DUT, can be used to offset the loss of dynamic range normally associated with pads. Selective use of external amplifiers with known gains, with or without pads, can even be used to augment dynamic range.

As noted above, there are no hardware adjustments in this VNA. Either the OSL or the Modified Response calibrations, depending on the measurement mode, is sufficient with the linear Detector in this VNA to provide all needed magnitude and phase information. Frequency calibration is established via adjustment of a software parameter after measuring the DDS output frequency against some known standard such as WWV.

Another feature to be noted in Figure 16, when combined with OSL or Response calibration, is that the test ports (reference plane locations) can be somewhat arbitrarily extended to provide powerful in situ or remote DUT measurement capability, such as shown in the antenna matching example.

For precise measurements of two-port or multi-port networks, any DUT port not connected to the VNA must be terminated in some standard impedance such as 50 Ω. This is necessary to be consistent with the definitions of S-parameters and their subsequent conversion to Y, Z, or H parameters.

Powering

Proper regulation of DC voltages used by the VNA is essential to its performance. The printed circuit board contains the low current, voltage regulators used to supply +5V and –5V to all PCB circuitry except for the signal sources.

The regulator for the +5V to the DDS signal sources and related circuitry is not present on the printed circuit board (PCB) due to the relatively high current requirements. Instead, the regulator is located on a separate external board where thermal management techniques can be best used and thereby minimizing its heating effects and possible coupled noise effects (in the case of a switching regulator) on the sensitive VNA circuitry. The PCB only contains a high frequency filter for the +5V to the DDS signal sources.

Performance Summary

This section summarizes the key characteristics of this VNA. Unless otherwise indicated, normal room ambient temperature is assumed. Due to limited hardware availability, typical measured values are shown.

There are some 2nd order thermal effects on Detector offset due to relatively small changes in DDS power dissipation with output frequency. As a result, frequency sweeps over narrow ranges may be slightly more accurate than sweeps done over wider ranges. Where applicable, narrowband or spot frequency testing was done in what follows.

Due to the broad range of options for bridges, their characteristics will not be included here, but in Part 2 instead.

Where applicable and possible, the format used here follows that of a typical commercial VNA [10].

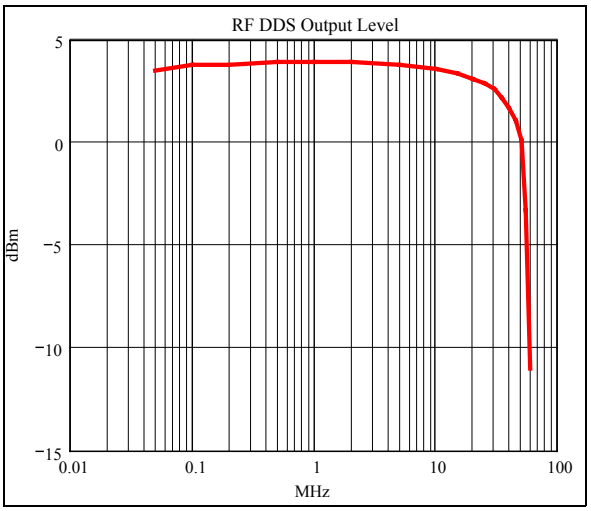
Master Oscillator(PCB Mount)

a) Frequency: 148.344 MHz
b) Type: 7th overtone BJT-FET Butler crystal oscillator
c) Output levels: CMOS compatible square wave, approx. 4.5 V pp minimum. centered on +2.5V DC, 45-55% duty cycle.
d) Loading: PCB traces, two 74AC74 Clk inputs, two AD9851 REFCLK inputs.

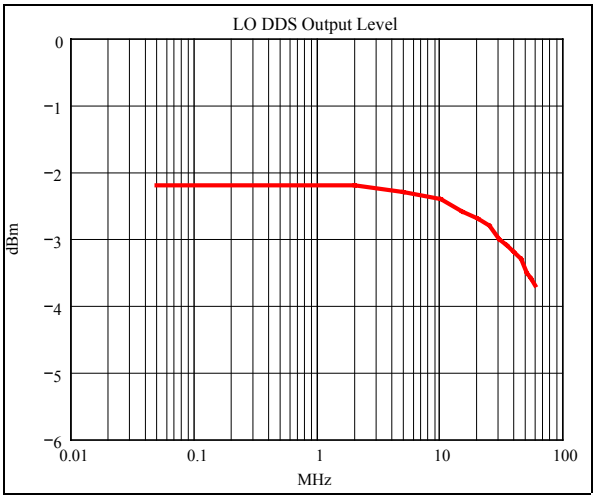
RF and LO DDSs

a) Frequency Range:
   1) VNA: 50 kHz – 60 MHz
   2) Usable: AC coupling limited, LO DDS is -3 dB at 0.2 Hz into a 1 Meg-Ω DC load. The RF DDS waveshape is limited by transformer saturation and is approx. sinusoidal down to 25 kHz with a 50 Ω load, lower frequency if more heavily loaded.
   3) RF and LO DDSs are independently frequency and phase programmable
b) Frequency resolution: approx. 0.035 Hz
c) Frequency Accuracy: +/-0.1 ppm with 10 MHz WWV, adjusted in software
d) Frequency Power-On Drift: -3 ppm or less
e) Frequency Temperature Coefficient: -0.1 ppm / °F or less after initial warm-up
f) Output levels @ 1 MHz into 50 Ω:
   1) RF DDS: 1.0 V pp (+3.9 dBm)
   2) LO DDS (each output): 0.5 V pp (-2.0 dBm)

g) DDS output level vs. Frequency:
RF DDS:

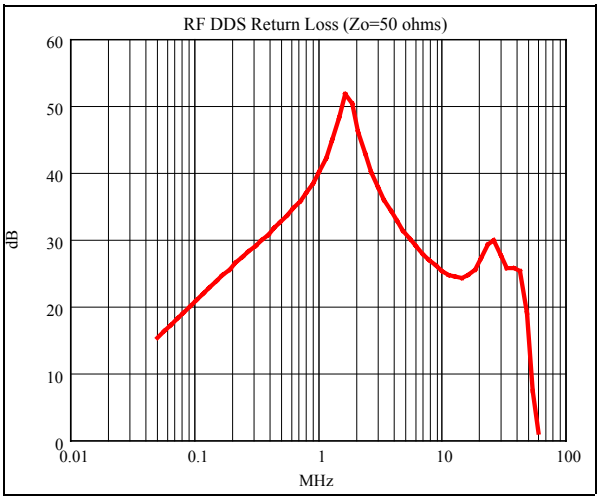


LO DDS filtered output (approx. 6 dB below RF DDS thru 30 MHz):

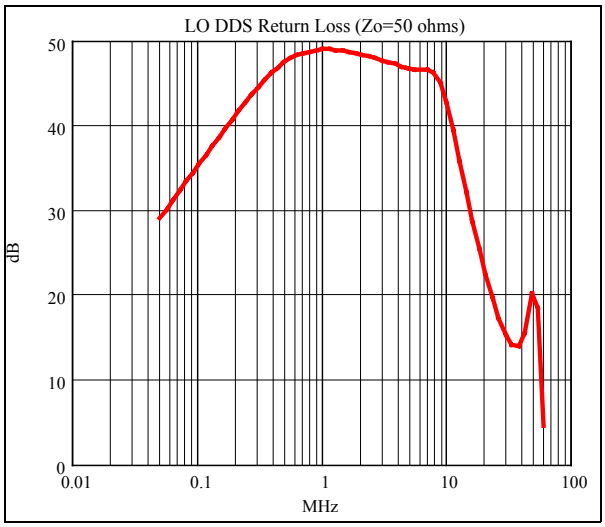


h) Nominal RF and LO Source Impedance: 50 Ω.

i) DDS Return Loss vs. Frequency @ F/SMA:
RF DDS:



LO DDS, filtered output:



j) RF DDS Spurious Outputs (50 Ω load):

1) Harmonics: -55 dBc or better, Fo=50-60 kHz
-60 dBc or better, 0.06-10 MHz
-50 dBc or better, 10-60 MHz
2nd harmonic dominant above 70 kHz

2) Aliases: -50 dBc or better, 0.05-45 MHz
-30 dBc or better, 45-60 MHz
-45 dBc @ Fo = Fmo/3 = 49.448 MHz

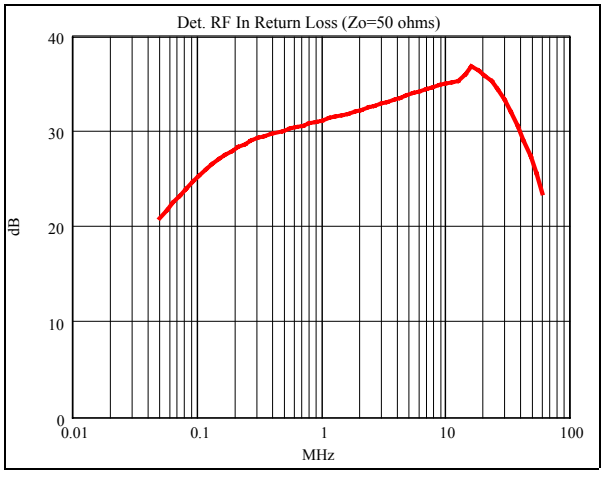
3) Other spurii: -70 dBc or better, 0.05-60 MHz

k) Phase Noise (measured at 10.2 MHz by W4ZCB)

Offset	dBc/Hz
100 Hz	-120
200	-120
300	-120
400	-130
500	-132
600	-134
700	-134
800	-132
900	-132
1 kHz	-136
2	-137
4	-141
5	-140
10	-142
50	-142
100	-121
101	-142

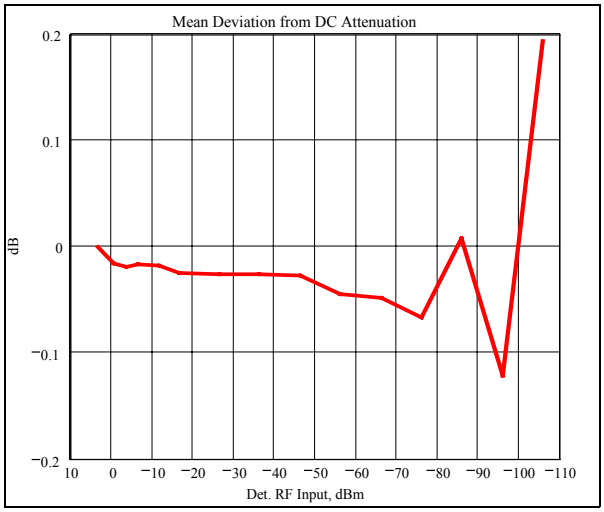
Detector

a) Type: Narrowband, linear, and direct convert to DC
b) Effective RF bandwidth: approx. 5 Hz
c) Gain: approx. 9 dB, rms at Det. RF In to DC out at the ADC input
d) Offset voltage: +/- 3 mV DC or less @ ADC input
e) ADC Input Range: -1.25 to +1.25 VDC
f) ADC Resolution: 24 bits
g) Effective Number of Bits: approx. 20
h) Conversions/sec: 7 (equivalent to 3.5 frequencies per second)
i) Maximum RF Input Signal: Approx. +5.5 dBm
j) Nominal RF and LO Input Impedance: 50 Ω
k) RF In Return Loss vs. Frequency @ F/SMA:

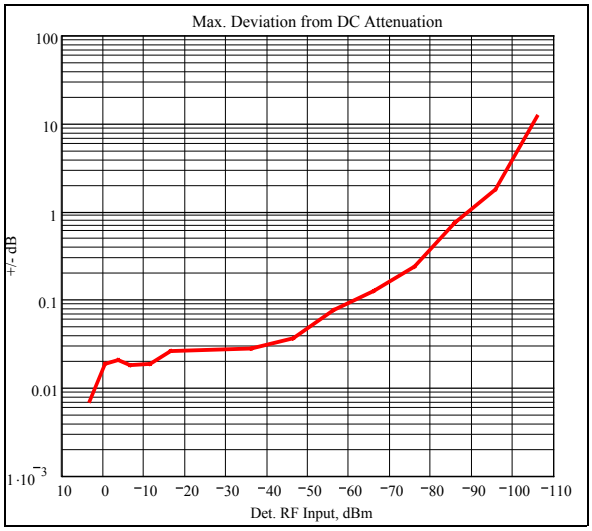


l) Magnitude Linearity, Accuracy, and Noise:
(Kay SMA 0-135 dB attenuator measurements @ 10 MHz with return losses of 38 and 40 dB)

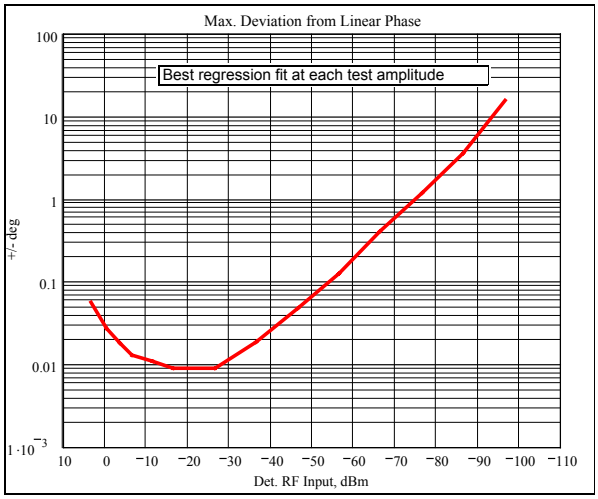
Mean of 32 samples:



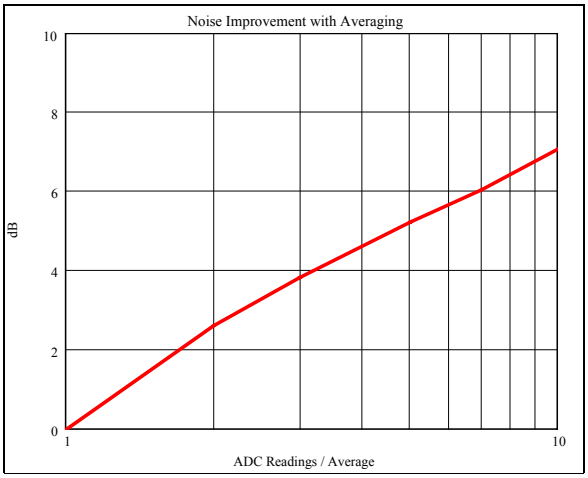
With noise (No averaging):



m) Phase Linearity, Accuracy, and Noise (same DUT as in l), no averaging):



n) Effect of averaging (noise limited):



o) Detector dynamic range (10 MHz):
114 dB, no averaging
121 dB, averaging 10 ADC readings

System Dynamic Range (10 MHz)

a) 112 dB, no averaging (Less in some cases depending on the DUT characteristics and harmonic mixing)
b) 119 dB, averaging 10 ADC readings:

Interface

Parallel Port on an IBM compatible PC, recommend use of an IEEE 1284 compliant parallel cable.

Control and Data Processing

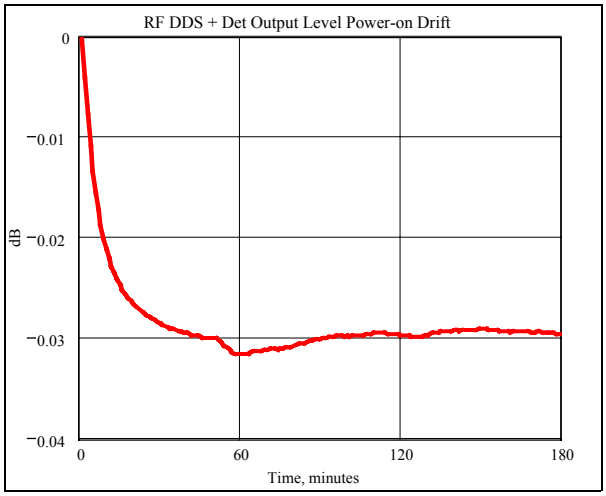
Software: DOS applications
Tested end use environments:
DOS, Windows 95, 98, and Windows 2000 with a virtual device driver such as Direct I/O [11].

Power Requirements

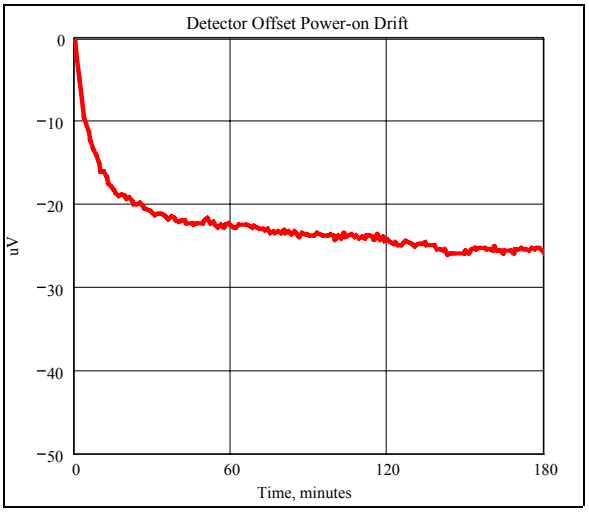
a) Input DC Voltages and Current:
+12 V (+9 V min. +15 V max) @ 25 mA and
+5.0 V +/-5% @ approx. 310 mA
b) +5V Ripple and Noise:
approx.1 mV pp broadband on scope, 15 uV rms at switcher fundamental frequency (50 kHz) on spectrum analyzer

Warm-up and Temperature Sensitivities

a) Detected RF DDS output level power-on drift:



b) Detector offset voltage power-on drift:



c) Detected RF DDS output level temperature coefficient:
-0.002 dB/°F after initial warm-up.
d) Detector offset temperature coefficient:
-1.9 uV/°F after initial warm-up

The measurement examples at the beginning that showed correlation to simulation models and/or nominal component values as well as the Kay attenuator measurements in the Detector Performance Summary provide some indication of VNA measurement accuracy.

The following will present methodologies to quantify accuracy in a more general fashion for transmission, reflection, and group delay measurements with this VNA.

Transmission Accuracy

Transmission accuracy is difficult to determine without a specific understanding of the DUT in question. It also depends on:

- Calibration technique and standards
- Source and Load Match
- Maximum usable DUT power
- Linearity
- Dynamic Range
- Signal/Noise ratio (noise floor)
- Averaging
- Repeatability (connectors)
- Drift (power-on and temperature)
- Variability (cabling)
- Analysis Method (RSS, Monte Carlo, or combination)

Armed with determinations for each of these, plus a calibration model, and an example DUT, a sample accuracy assessment will be made on what follows. The method presented here also permits a user to make accuracy estimates for other DUTs and parameter assumptions that may be of interest.

a) Calibration Technique: A modified response calibration is used where a Thru line is used to establish the unity gain at zero phase plus an open (or terminated) Detector RF input is used to establish the zero signal level.
b) Calibration Model. The following equations were derived for the modified response calibration used in this VNA:

$$G_m := \frac{S_{21}\cdot\left(1-\Gamma_L\cdot\Gamma_S\right)}{\left(1-S_{22}\cdot\Gamma_L\right)\cdot\left(1-S_{11}\cdot\Gamma_S-\frac{S_{21}\cdot S_{12}\cdot\Gamma_L\cdot\Gamma_S}{1-S_{22}\cdot\Gamma_L}\right)}$$

or equivalently

$$G_m := \frac{S_{21}\cdot\left(1-\Gamma_L\cdot\Gamma_S\right)}{\left(1-S_{22}\cdot\Gamma_L\right)\cdot\left(1-S_{IN}\cdot\Gamma_S\right)}$$

where

G_m is the measured complex voltage insertion gain,
S_{11} – S_{22} are the DUT S-parameters,
Γ_S and Γ_L are respectively the Source and Load Match of the VNA test ports at the DUT terminals.
S_{IN} is the reflection coefficient at port 1 with Γ_L terminating port 2.

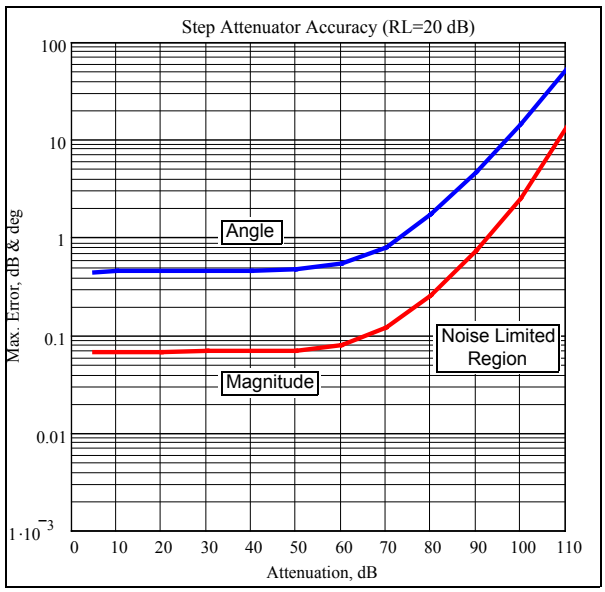
Note that these are vector equations that permit angle error in G_m to be determined in addition to magnitude error. These equations show that G_m will approximate S_{21} of the DUT if Γ_S and Γ_L are both nearly zero, i.e. if the source and load impedance are both approx. 50 Ω. The equations also show that the DUT S-parameters also affect the degree of interaction or coupling due to matching errors at the VNA test ports.

Also critical to this analysis are assumptions regarding the rotation of error vectors. The standard assumption of arbitrary rotation to force worst-case additions or subtractions is valid for microwave frequencies, but possibly not at 50 kHz and into the lower HF range.

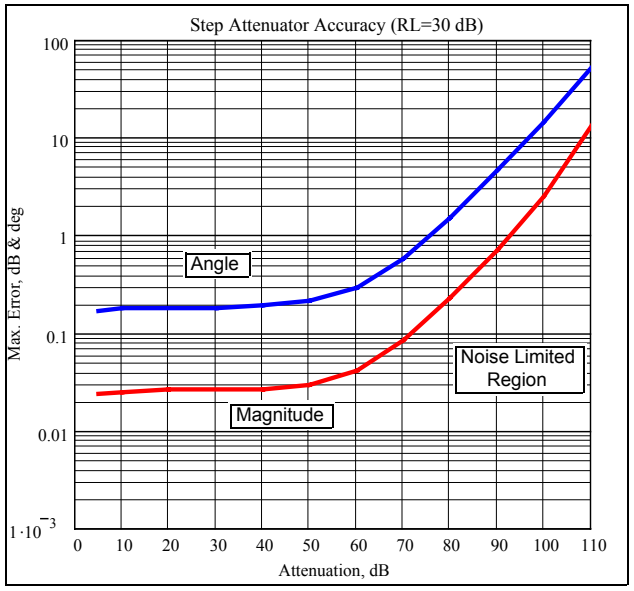
Since the source and load impedance are both approx. 50 Ω, G_m errors will be normalized to S_{21} in this example.

c) Analysis method: While Root Sum Square (RSS) is commonly used [12], an earlier Monte Carlo type statistical method [13] is used here. The Monte Carlo method allows the user to control the angles used for the various error vectors and also to determine the confidence level.
d) Averaging: None
e) Repeatability and Stability: Assumed negligible
f) Drift: Assumed negligible
g) Frequency: 10 MHz
h) DUT: Nominal 50 Ω 0-110 dB step attenuator with return losses exceeding 20 dB or 30 dB, 0 dB used as thru calibration standard, DUT is 5, 10, 20,…100, 110 dB
i) DUT input power: approx. +4 dBm
j) System dynamic range: 112 dB
j) Vectors:
   Γ_S: 0.054 @ -152° (measured with 2nd VNA)
   Γ_L: 0.022 @ 82° (measured with 2nd VNA)
   S_{11}: 0.10 or 0.032 @ 0 to 360°, uniformly distributed
   S_{21}: magnitude per DUT attenuations above @ 0°
   $S_{12} = S_{21}$
   S_{22}: 0.10 or 0.032 @ 0 to 360°, uniformly distributed
k) Noise: Treated as a vector of constant magnitude with its phase as a random variable between 0 and 360° selected in the Monte Carlo algorithm. Its magnitude is scaled to S_{21} based on the DUT input power and the system dynamic range.
l) G_m Error with respect to S_{21}:

Attenuator Return Loss = 20 dB:



Attenuator Return Loss = 30 dB:



The errors seen here at 10 MHz will be larger at the 50 kHz and 60 MHz end frequency limits due to increased Γ_S as seen in the RF DDS return loss plot. However, the error at the end frequencies can be reduced with the addition on the source side of either external pads or a pre-amp with an attenuator at its output.

More reflective devices, such as filters entering stopband, will also have greater G_m errors. Also, if the source and load match is degraded with external cabling or amplifiers, then the G_m error will again be larger.

Reflection Accuracy

Many of the dependencies listed for transmission accuracy also affect reflection accuracy. Reflection accuracy depends more critically on the quality and accuracy of the calibration standards used. However, most of the other systematic errors, such as directivity. tracking and source and load match, are eliminated with the Open, Short, Load (OSL) calibration method that is used in this VNA.

With calibration standards of known accuracy, what is generally done [14] is to supply the needed data to a

calibration model and determine what are called “residual errors.” These residual or corrected errors are commonly quoted in a VNA specification.

Without purchased or NIST traceable calibration standards, the process described in [14] is nearly impossible but can be pursued with appropriate standards.

Since calibration standards were not purchased nor were NIST traceable standards directly available, results of a correlation test with a commercial VNA with NIST traceable standards are presented here instead. Fortunately, this correlation activity also demonstrates that good quality SMA calibration standards can be constructed and used for the 0.05 – 60 MHz range. These calibration standards also have good accuracy through 1 GHz.

This activity was provided by me using my VNA and by Chip Owens, NWØO, using a commercial VNA. Chip’s data collection proved to be more time consuming than first anticipated. I am extremely grateful to Chip for the time and effort that he expended in collecting this data.

a) VNAs:
   - Paul: N2PK VNA
   - Chip Agilent 8753C [15]

b) Bridges:
   - Paul: Wheatstone with a Mini-Circuits T1-1T transformer to VNA Detector
   - Chip: Agilent 85046A [16]

b) Calibration technique: Open, Short, Load (OSL)

c) Calibration standards:
   - Paul: Three Amphenol, PN 901-144-9RFX, SMA jacks with the center pin ground down flush with the dielectric at the back of the connector are used for each of the OSL calibration standards.
     The Open is an SMA jack as above.
     The Short is an SMA jack as above with a flat foil disk soldered to the center conductor and the entire periphery of the outer conductor and in contact with the teflon dielectric.
     The 50 Ω load is an SMA jack as above with two 100 Ω, 0603, +/-0.1% resistors mounted diametrically opposed and each soldered to the center and outer conductors of the SMA and in contact with the teflon dielectric.
     Very small amounts of Ambroid liquid cement were used to aid in mechanically securing the SMA center conductor on the Open and the resistors on the 50 Ω load.
   - Chip: Agilent 85033C 3.5 mm cal kit. SMAs can be mated with 3.5 mm connectors.

d) DUT and its construction:
   Series RC load on an Amphenol SMA jack same as my calibration standards construction. Consists of an 0805 SMD 24.9 Ω 1% resistor and two 0805 100 pf 5% NPO capacitors in parallel.

d) Method:
   - Paul: Used my calibration standards and measured DUT at spot frequencies of 1, 10, 20, …50, 60 MHz
   - Chip: Used 85033C jack calibrations standards and measured my calibration standards and the DUT at the above spot frequencies plus higher frequencies through 1 GHz.

e) Source power @ DUT:
   - Paul: 6 dB down from RF DDS level, or approx. -2 dBm up to 10 MHz dropping to –17 dBm @ 60 MHz
   - Chip: -23 dBm

f) Nominal reference plane locations:
   - Paul: The back of the SMA jack flush with the dielectric.
   - Chip: Outer conductor mating surface on 3.5 mm connectors which nearly corresponds to the front of the SMA jack flush with the dielectric.

g) Reference plane offset:
   Based on Chip’s 1 GHz measurement of my short, there is a 34.2 ps offset between our reference plane locations. This offset is used as needed to correct one or the other set to compare data at the same plane.

h) Chip’s data for my calibration standards:
   Unfortunately, there were some erratic results during the test of my calibration standards that Chip later traced to a faulty cable in his VNA. Here are data that do not appear to have been affected:
   Open:

F	|rho|	<rho	Corr. <rho
4Ø	1.ØØ1	-1.Ø5	-Ø.Ø6
5Ø	1.ØØ1	-1.28	-Ø.Ø5
6Ø	Ø.999	-1.58	-Ø.1Ø
7Ø	Ø.998	-1.87	-Ø.15
8Ø	Ø.999	-2.Ø6	-Ø.Ø9
9Ø	Ø.999	-2.29	-Ø.Ø8
1ØØ	Ø.999	-2.62	-Ø.16
146	1.ØØØ	-3.81	-Ø.22
5ØØ	1.ØØØ	-13.Ø5	-Ø.74
1ØØØ	1.ØØØ	-25.98	-1.36

The corrected angle data above in degrees accounts for the 34.2 ps offset in reference plane locations. It can be used to project an open fringing capacitance of Ø.ØØ39 pF.

Short:

F	|rho|	<rho	Corr. <rho
4Ø	Ø.998	178.9Ø	179.88
5Ø	Ø.997	178.7Ø	179.93
6Ø	Ø.998	178.4Ø	179.88
7Ø	Ø.998	178.2Ø	179.92
8Ø	Ø.998	177.9Ø	179.87
9Ø	Ø.997	177.7Ø	179.92
146	Ø.998	176.38	179.98
5ØØ	Ø.997	167.67	179.98
1ØØØ	Ø.997	155.38	18Ø.ØØ

The 1 GHz angle data above was used to determine the 34.2 ps offset in reference plane locations and the corrected angles at the other frequencies as a result.

50 Ω load:

F	Ret.Loss dB	<rho	Corr. <rho
3Ø	62.8	119.5	12Ø.3
4Ø	68.2	167.4	168.3
5Ø	62.1	131.1	132.4
6Ø	64.9	164.2	165.7
7Ø	67.2	-164.8	-163.1
8Ø	62.8	167.7	169.7
9Ø	59.5	163.6	165.8
1ØØ	62.4	158.3	16Ø.8
146	6Ø.7	134.Ø	137.5
5ØØ	51.Ø	94.4	1Ø6.7
1ØØØ	45.4	79.3	1Ø3.9

Chip also evaluated three other resistor configurations including 4x200-Ω and found the above to be the best for return loss through 1 GHz.

i) Common DUT data comparison:

Adjusting my reflection data to the front of the SMA jack to correspond to Chip's reference plane results in:

	|rho|			angle rho, deg		
F	Paul	Chip	Delta	Paul(cor)	Chip	Delta
1	Ø.9961	Ø.997Ø	-Ø.ØØØ9	-7.15	-7.19	Ø.Ø3
1Ø	Ø.7641	Ø.7643	-Ø.ØØØ2	-6Ø.82	-6Ø.8Ø	-Ø.Ø2
2Ø	Ø.5541	Ø.5537	Ø.ØØØ4	-94.7Ø	-94.72	Ø.Ø2
3Ø	Ø.4575	Ø.4565	Ø.ØØ1Ø	-114.85	-115.Ø7	Ø.22
4Ø	Ø.41Ø2	Ø.41Ø7	-Ø.ØØØ5	-128.24	-128.27	Ø.Ø3
5Ø	Ø.3846	Ø.3838	Ø.ØØØ8	-137.72	-137.9Ø	Ø.18
6Ø	Ø.3695	Ø.3687	Ø.ØØØ8	-144.79	-144.9Ø	Ø.11

and adjusting Chip's reflection data to the back of the SMA jack to correspond to my reference plane location

	Rs, Ω			Cs, pF		
F	Paul	Chip	Delta	Paul	Chip	Delta
1	25.2Ø	19.25	+5.95	198.6	199.3	-Ø.7
1Ø	24.98	24.97	+Ø.Ø1	199.2	199.1	+Ø.1
2Ø	24.96	24.97	-Ø.Ø1	199.9	2ØØ.1	-Ø.2
3Ø	24.97	24.98	-Ø.Ø1	2Ø1.1	2Ø2.1	-1.Ø
4Ø	24.98	24.95	+Ø.Ø3	2Ø2.9	2Ø2.9	Ø.Ø
5Ø	24.98	25.ØØ	-Ø.Ø2	2Ø5.Ø	2Ø6.2	-1.2
6Ø	24.97	25.ØØ	-Ø.Ø3	2Ø7.8	2Ø8.6	-Ø.8

Note that the difference in Rs at 1 MHz is mostly the result of a 0.0078 dB difference in return loss!

Correcting my Cs data using a stray Ls = 1.5 nH results in Cs' = 198.9 +0.2 /-0.3 pF.
Correcting Chip's Cs data using a stray Ls = 1.6 nH results in Cs' = 199.2 +0.5/-0.4 pF.

Group Delay Accuracy

Generally, group delay accuracy depends on the rate of change of the transmission phase errors with frequency. While it is possible to use the transmission error methodology and apply it to two relatively close frequencies as typically used in a group delay calculation, the typical DUT of interest for group delay is a filter and the rate of change in phase error will depend on both its transmission and reflection dependencies on frequency which appear to be difficult to specify in any generally meaningful way.

Notes

Clicking on a URL below with an active Internet connection, in most cases, will bring it up in your web browser if you have the Adobe plug-in. If any documents cannot be found (the web is a dynamic place), please contact me by e-mail.

1. For a detailed treatment of vector network analyzer principles, see the Agilent (previously HP) AN 1287-X series of application notes at:
   http://cp.literature.agilent.com/litweb/pdf/5965-7707E.pdf (1287-1)
   http://cp.literature.agilent.com/litweb/pdf/5965-7708E.pdf (1287-2)
   http://cp.literature.agilent.com/litweb/pdf/5965-7709E.pdf (1287-3)
   http://cp.literature.agilent.com/litweb/pdf/5965-7710E.pdf (1287-4)
   There are six additional app notes in this series that may also be of interest and can be found by searching:
   http://www.agilent.com
2. For an overview of VNA basics, see the series of slides at
   http://cp.literature.agilent.com/litweb/pdf/5965-7707E.pdf
3. An overview of direct digital synthesis can be found at
   http://www.analog.com/UploadedFiles/Tutorials/540111891100165151833435330791040025 17DDStutor.pdf
4. A description of the AD9851 DDS 1X and 6X REFCLK timing requirements can be found at
   http://www.analog.com/UploadedFiles/Application_Notes/599711852800924681833359689AN-587.pdf
5. For a return loss bridge, see *The ARRL Handbook*, 78th Edition(2001), p. 26.42, Fig C.
6. The Mini-Circuits PSC-2-1W power splitter can be found at:
   http://www.minicircuits.com/cgi-bin/spec?cat=splitter&model=PSC-2-1W&pix=a01.gif&bv=4
   When used as a bridge, the *Sum* port is the DUT port.
7. The Mini-Circuits PDC-10-1 directional coupler can be found at
   http://www.minicircuits.com/cgi-bin/spec?cat=coupler&model=PDC-10-1&pix=a01.gif&bv=4
8. Descriptions of the two transformer directional coupler, as used in the Stockton bridge and Tandem Match coupler, can be found in
   Wes Hayward, W7ZOI, "Introduction to Radio Frequency Design," 1st ARRL Edition, p 156-158.
   John Grebenkemper, KA3BLO, "The Tandem Match - An Accurate Directional Wattmeter," *QST,* Jan 1987, pp 18-26.
   The Tandem Match also appears in various editions of *The ARRL Handbook* and *The ARRL Antenna Handbook*,
   Paul Kiciak, N2PK, "An HF In-Line Return Loss and Power Meter," The QRP Quarterly, October 2002, p 17-25.
9. A detailed treatment of VNA calibration standards can be found at:
   http://cp.literature.agilent.com/litweb/pdf/5956-4352.pdf
   A description of the *Reference Plane* is on page 3, while the *Calibration Plane* is on pages 8 and 26-27.
10. The specification for the Agilent 8753ES is available at:
    http://cp.literature.agilent.com/litweb/pdf/5968-5160E.pdf
11. Direct I/O for Windows 2000 can be found at:
    http://www.direct-io.com/
    Although currently untested, the VNA software may work with Direct I/O in Windows NT and XP.
12. See Section 10 of Agilent's Reference Guide for the 8753ES and 8753ET Network Analyzers at:
    http://cp.literature.agilent.com/litweb/pdf/08753-90473.pdf
13. B. P. Hand, "Developing Accuracy Specifications for Automatic Network Analyzer Systems," Hewlett-Packard Journal, Feb. 1970.
14. Godfrey Kwan, "Sensitivity Analysis of One-port Characterized Devices in Vector Network Analyzer Calibrations: Theory and Computational Analysis," available at:
    http://metrologyforum.tm.agilent.com/pdf/NCSLI2002_kwan.pdf
15. The Agilent 8753C is now obsolete and replaced by the 8753ES . The datasheet for the 8753D is at:
    http://cp.literature.agilent.com/litweb/pdf/5962-9770E.pdf
16. The datasheet for the Agilent 85046A Test Set is at:
    http://cp.literature.agilent.com/litweb/pdf/5952-2765.pdf