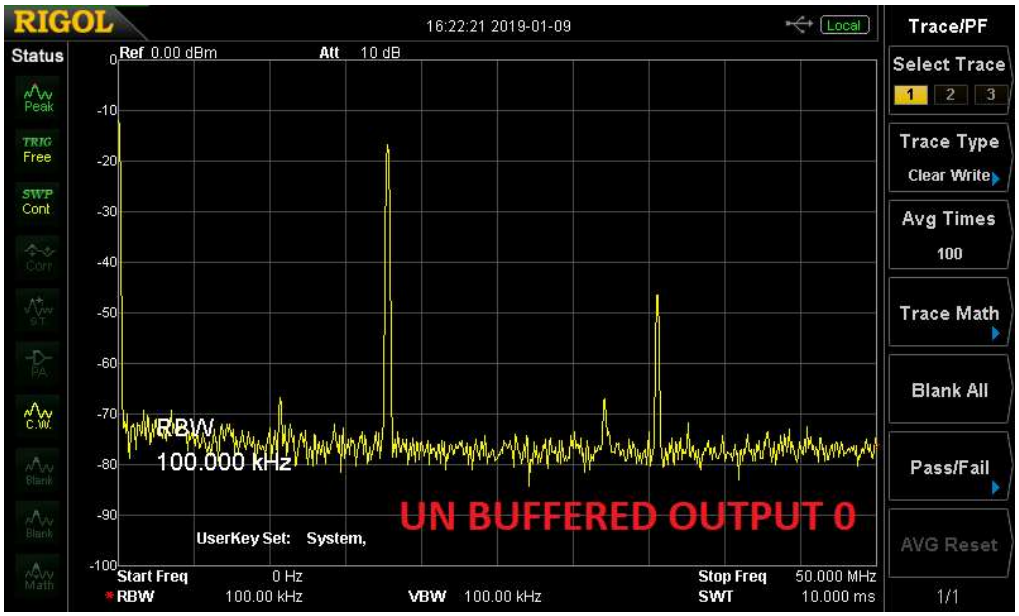
Si5351 Buffering

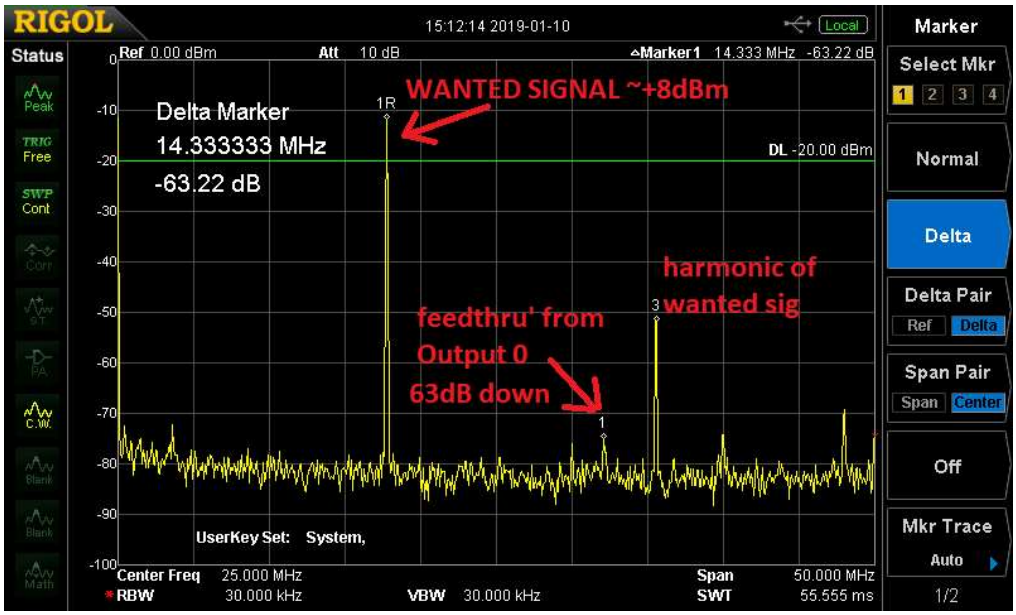
This is a comparison of a Si5351 board that is not buffered, compared to one with buffering, via a single gate logic device per channel. (ie 3 x 74LVC1G04GW) An SA is used as the 50 ohm load and measuring instrument. The connection to SA was at the outputs, each having a series 47R resistor inline.

In both cases output 0 is programmed to ~10.7MHz and output 2 to ~17.7MHz (for the BFO and VFO in a 40M SSB receiver)

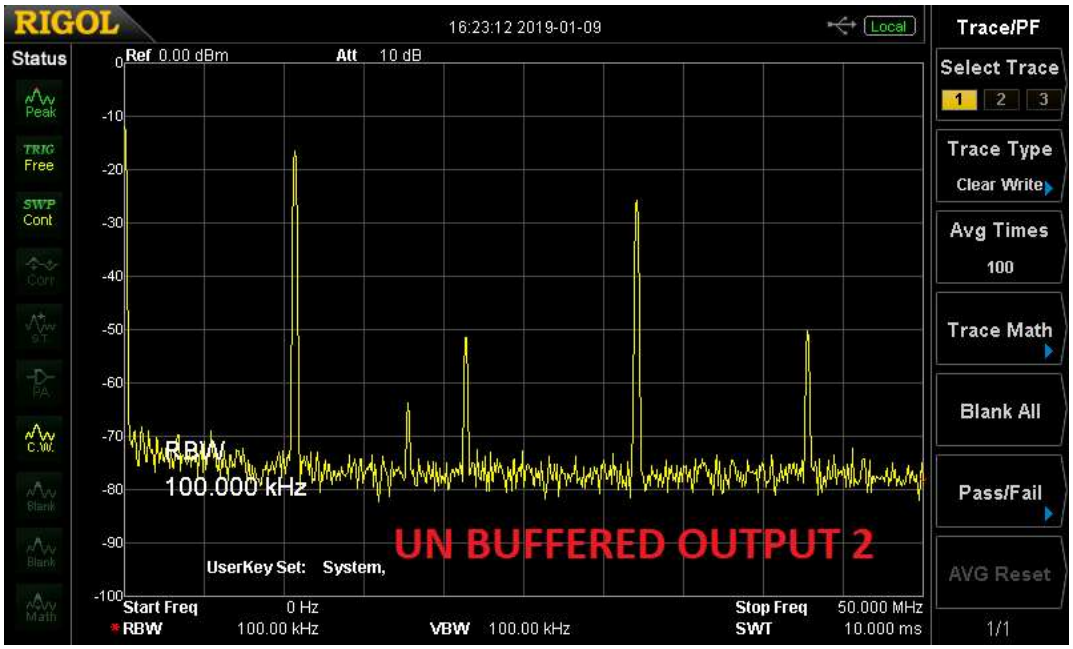
This is the unbuffered output 0. The stronger signal is the wanted 17.7MHz at a level of ~+4dBm (a 20dB pad is used into the SA). The next larger signal is 2nd harmonic. The two low level signals are feedthrough from the other used output, 1. They are approx.. 50dB down.



Below, is the same signal but from the buffered board. The wanted signal is now ~+8dBm. The unwanted signals from output 1 are now down approx. 63dB. A >10dB improvement. 2nd harmonic is reduced also.



Next we check output 2 on the unbuffered board, below. The wanted signal at ~10.7MHz is at a level of about +4dBm. The feedthrough from output 0 is the next signal. It's about -42dB down



This the buffered output 2, below. The feedthrough from output 0 is now about -58dB down. Around 16dB better when buffered. The other strong signals are harmonics of the wanted output signal of 10.7MHz. The green horizontal line is 0dBm reference line.

So, with buffering in these test examples, we get output level more suited to a double balanced diode mixer and improved suppression of the other channel by at least 10dB.

Tested 9th Jan 2019 by VK3PE